University of Alberta

Radiation-Tolerant Design with 0.18-micron CMOS Technology

by

Li Chen ©

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This thesis is dedicated to my son Alexander and my wife Qibing.

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List of Symbols

Symbol	Description	Unit
C_d	Depletion-layer capacitance per unit area	F/cm^2
C_{it}	Interface trapped capacitance per unit area	F/cm^2
C_{ox}	Oxide capacitance per unit area	F/cm^2
ΔN_{ot}	The areal trapped charge density referred to the SiO$_2$-Si interface	C/cm^2
ΔV_T	Threshold voltage shift	V
ΔV_{it}	Threshold voltage shift introduced by the charge trapping in the interface	V
ΔV_{ox}	Threshold voltage shift introduced by the charge trapping in the silicon oxide	V
ε_{ox}	Oxide permittivity (= 3.45 × 10^{-13} F/cm)	F/cm
f	Frequency, clock frequency	Hz
ϕ_B	Bulk potential	V
ϕ_t	Thermal voltage (=0.0259 V, when 300°K)	V
g_d	MOSFET small-signal output conductance	A/V
g_m	MOSFET small-signal transconductance	A/V
g_{mb}	MOSFET small-signal bulk transconductance	A/V
I_d	Drain Current in a MOSFET	A
K_B	Boltzmann's constant (= 1.38 × 10^{-23} J/K)	J/K
L	Length, MOSFET channel length	cm
L_{eff}	Effective channel length	cm
λ	Channel length modulation	1/V
μ	Carrier mobility	cm^2/V-s
μ_0	Pre-radiation carrier mobility	cm^2/V-s
n_i	Silicon intrinsic carrier density	cm^{-3}
q	Electronic charge (= 1.6 × 10^{-19} C)	C
Q_c	Critical charge for single-event upset	C

r	Resistance	Ω
R_B	MOSFET substrate resistance	Ω
R_G	MOSFET polysilicon gate resistance	Ω
ρ	Sheet resistance	Ω/square
s	Second	second
S	MOSFET subthreshold slope	V/decade
t_{ox}	Oxide thickness	cm
T	Absolute temperature	K
V	Voltage	V
V_{bs}	MOSFET substrate voltage	V
V_{ds}	MOSFET drain voltage	V
V_{dd}	Power supply voltage	V
V_{dsat}	MOSFET drain saturation voltage	V
V_{gs}	MOSFET gate voltage	V
V_T	Threshold voltage	V
W	MOSFET width	cm

List of Abbreviations

Abbreviation	Description
APD	Automatic power down
ASIC	Application-specific integrated circuit
ATD	Address transition detector
CAD	Computer-aided design
CERN	The European Organization for Nuclear Research
CMOS	Complementary metal-oxide-semiconductor
COTS	Commercial-off-the-shelf
CPU	Central processing unit
CSR	Centre for Subatomic Research
DDWL	Dynamic divided word line
DEAC	Error detection and correction
DICE	The dual interlocked storage cell
DRAM	Dynamic random-access memory
DUT	Device under test
ELT	Enclosed-gate layout transistor
EMP	Electromagnetic pulse
FPGA	Field-programmable gate array
IC	Integrated circuit
LET	Linear energy transfer
LHC	The large hadron collider
LOCOS	Local oxidation of silicon
MBU	Multiple bit upset
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field effect transistor
NMOS	N-channel metal-oxide-semiconductor
PMOS	P-channel metal-oxide-semiconductor
SCR	Silicon-controlled rectifier
SEBO	Single-event burn out

SEE	Single-event effect
SEFI	Single-event functional interrupt
SEL	Single-event latch-up
SEU	Single-event upset
SEGR	Single-event gate rupture
SHE	Single hard error
SOI	Silicon on insulator
SOS	Silicon on sapphire
SRAM	Static random-access memory
STI	Shallow-trench isolation
TID	Total ionizing dose effect
TSMC	Taiwan semiconductor manufacturing company
VLSI	Very large-scale integration

Introduction

Almost forty years ago, the effects of radiation on semiconductor devices were observed when the first satellite experienced serious problems caused by the high energy particles present in the Van Allen belts [Spj83]. Since then, the space and military communities have made efforts to study these effects on semiconductors. Currently, the interest in studying circuits that can work in a radiation environment is increasing, driven by all the possible applications of this kind of technology, such as space missions, satellites, advanced weaponry, instrumentation for nuclear power plants and high-energy physics experiments. With the evolution of very large-scale integration (VLSI) technologies, the minimum feature size of a transistor is becoming smaller and smaller; at the same time, scientists have become aware that the radiation effects caused mainly by neutrons can no longer be ignored in VLSI devices even at ground level. These radiation environments will be discussed in chapter one.

Custom-designed radiation-tolerant and hard technologies[1] have been developed by the space and military communities, by using foundry-oriented solutions. The disadvantages of these solutions are that they are expensive, difficult to access and normally several generations behind current commercial technologies.

The part of MOS (metal-oxide-semiconductor) transistors that is the most sensitive to ionizing radiation effects is the gate oxide, as will be seen in chapter two. The charges induced by ionizing radiation are trapped in the oxide, which precludes the traditional thick-oxide commercial technologies from being used in radiation environments. One way to reduce the effects of ionizing radiation in the gate oxide is to reduce its thickness, which is fortunately a natural trend in modern technologies. The market for computer memories, microprocessors and, in general, digital integrated circuits has driven a very fast technological evolution over the past 20 years which has led to today's deep submicron technologies with less than 5 nm gate oxide thickness [Ane99]. The inherent radiation tolerance of the gate oxide of modern commercial CMOS (Complementary MOS) technologies suggests the possibility of using them in a radiation environment without introducing or modifying any particular process step. This will be seen in chapter 3. Radiation hardening a technology by introducing special processing steps is generally not a convenient way to proceed since the foundries will not modify their processes for a small market without raising prices considerably.

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[1] Radiation-hard normally refers to a higher level of radiation hardness than radiation-tolerant [CER].

There are some other possible problems besides the gate oxide when irradiating an integrated circuit made in a standard deep submicron technology. The scaling down of CMOS technologies also brings some detrimental effects. It is necessary to adapt the layout and the architecture of the circuits and of the system to solve these problems. A specially shaped transistor called the enclosed-gate layout transistor (ELT, also called enclosed-gate transistor) as well as guard rings are introduced.

The European Organization for Nuclear Research (CERN) started to investigate the possibility of using a commercial CMOS technology to integrate the circuits to be used in the detectors of high-energy physics experiments. They studied MOS devices fabricated using 0.7 μm, 0.5 μm, and 0.25 μm technologies. Some layout techniques were also studied to increase their radiation tolerance. The results were very promising, as reported in the RD49 project Status Reports [RD49a, RD49b]. The successful results allowed the design of integrated circuits, that could withstand total doses of 300 kGy(SiO_2) and beyond [Cam99, Jar99, Sno00].

With CMOS technologies scaling down, 0.18-μm and 0.13-μm CMOS processes have become the mainstream technologies used in commercial products. Radiation hardness perspectives for the design of analog detector readout circuits in 0.18-μm CMOS technology have been investigated by some researchers [Man02]. This work shows that the increase of the leakage component in the NMOS drain-source current may affect the behavior of devices used for logic or switching functions in radiation environments. Some layout techniques (ELTs and guard rings) have been used to cure this problem. However, the characteristics of enclosed-gate layout transistors in radiation environments have not been studied thoroughly yet, and this prohibits them from being used in radiation-tolerant applications. For example, the use of short channel transistors in analog sections requires knowledge of parameters such as transconductance and noise, which may differ considerably from the theoretical predictions valid for long-channel devices. The radiation tolerance of these analog parameters is also an important issue in electronic circuits for detectors in high-energy physics. A 0.18-μm CMOS technology is used in this thesis. This thesis reports work done in the development of a radiation-tolerant layout approach. A model to calculate the effective aspect ratio of enclosed-gate layout transistors is introduced and verified. The transistor parameters are extracted, before and after irradiation, to study the radiation hardness of the technology. A digital library with enclosed-gate transistors has been developed and a SRAM test chip has been designed and fabricated. Techniques to design radiation-hard SRAM cells are also introduced and evaluated. Some techniques used to prevent single-event upset in a SRAM are also evaluated using the technology. These approaches, which are used to make them radiation-tolerant, have general validity. For example, they could be used in radiation-hard circuits for space, military and other radiation applications, besides high-energy physics experiments.

A description of the contents of the thesis, chapter by chapter, follows:

- Chapter 1: This chapter introduces the different radiation environments, which have radiation effects on semiconductor devices. These include the space environment, the ground level environment, the nuclear reactor environment, the radiation processing environment, the weapons environment and high-energy physics experiments.

- Chapter 2: This is an introductory section describing the radiation effects on semiconductors. There are two major effects on MOSFETs, namely, total ionizing dose effects (TID) and single-event effects (SEE). The physical origin of the MOS transistor parameters degradation induced by the total radiation dose is discussed together with the single-event effects. MOS devices are not sensitive to displacement damage, so no detailed information is given for this effect. This chapter is fundamental to understanding the rest of the thesis.

- Chapter 3: The first part of this chapter introduces the scaling laws of CMOS technologies. Both beneficial and detrimental radiation effects of the technology scaling are presented.

- Chapter 4: Different levels of radiation-hardening techniques are discussed in this chapter. Traditionally, radiation hardening is achieved by using radiation-hard foundries, which are generally used for space and military purposes. However, radiation hardening can also be achieved by using design techniques. At the transistor level, there are enclosed-gate transistors and guard rings. Various circuit and system-level design techniques are introduced in this chapter.

- Chapter 5: ELTs are devices with an enclosed-gate geometry, with the drain and source contacts inside and outside, separated by a gate ring. They are used to prevent post-irradiation leakage currents between drain and source inside the NMOS transistors. In this chapter the work done on the modeling of these non-standard geometry devices is described.

- Chapter 6: Total dose effects on ELTs are thoroughly studied. The radiation hardness of MOSFETs in the technology with a gate oxide thickness of 4.3 nm and with an enclosed gate and guard ring layout has been evaluated based on its electrical characteristics. Some important parameters have been measured or extracted in this chapter.

- Chapter 7: Noise is an important parameter in analog CMOS circuits. Radiation may affect the noise behavior of the devices. It is mandatory to evaluate the noise performance of standard and ELT transistors before and after radiation in order to use them in analog circuits.

- Chapter 8: A digital library is developed with ELTs and guard rings. A configurable SRAM architecture is introduced aimed at radiation-hard ASIC designs. Some low-power techniques have been adopted. A 1k × 9 bit SRAM test chip has been designed and fabricated with the technology.

- Chapter 9: Single-event upset in memories is studied in this chapter. Several approaches to radiation-hardened SRAM cells are introduced and evaluated using the technology.

- Conclusions: The main results and their significance are discussed, together with their possible applications in radiation environments.

Chapter 1 Introduction to Radiation Environments

In this section, a brief overview of the various environments likely to have a degrading effect on electronic devices and systems is presented. The environments include space, ground level, nuclear reactors, radiation processing, weapons and high-energy physics experiments.

1.1 The space environment

The space radiation environment is composed of a variety of energetic particles with energies ranging from keV to GeV and beyond [Sta88]. These particles are either trapped by the Earth's magnetic field or are passing through the solar system. The main elements of the radiation environment are the radiation belts, cosmic rays, and solar flares.

- The radiation belts. This consists of many different types of energetic charged particles trapped in the Earth's magnetic field, forming the radiation belts. The belts consist mainly of electrons of energy of up to a few MeV and protons of up to several hundred MeV.

- Cosmic rays. These are low fluxes of energetic heavy ions extending to energies beyond TeV and including all ions in the periodic table. There are three sources of cosmic rays: galactic, solar and terrestrial. Galactic cosmic rays are 'primary' cosmic rays which originate from outside the solar system but are associated with the galaxy and provide a continuous low-flux component of the radiation environment. They are comprised of about 85 per cent protons, 14 per cent alpha particles and 1 per cent heavier nuclei with energies extending to 1 GeV. Solar cosmic rays not only produce an intensive burst of both UV and X-rays, but also accelerate solar material to high velocities. These solar particles are similar to galactic cosmic rays but, due to their different origin, are not identical in composition. The primary cosmic radiation which penetrates the Earth's atmosphere is rapidly transformed by interactions which produce a cascade of secondary radiation. These cascades take place in the main body of the atmosphere and the secondary particles produced are the principal components of cosmic radiation at the Earth's surface, which are called terrestrial cosmic rays.

- Solar flares. Protons from solar flares, together with electrons, alpha particles, and photons in smaller quantities, are emitted by the sun in bursts during solar storms. Their fluxes, besides being intermittent, vary overall with the solar cycle.

In addition, space is pervaded by a plasma of electrons and protons with energies up to about 100 keV. Within the trapped radiation belts, these particles merely represent the low-energy extremes of the trapped electron and proton populations. In the outer zones of the magnetosphere and in interplanetary space, these particles are associated with the solar wind, and considerable fluxes will be encountered at very high altitudes. The low-energy particles are easily stopped by very thin layers of material and hence only the outermost surfaces, such as thermal control material and solar cell cover slips, are affected. The low-energy plasma can cause spacecraft charging and the internal electronics may be affected by this charging and subsequent discharging.

Electronics in space experiences two types of radiation effects: one is caused by the accumulation of ionization over a period of time, which eventually leads to performance degradation and/or functional failure. The other one is due to a single high-energy particle as it strikes the sensitive nodes (or sensitive volumes) within the electronic device. It is primarily the results of currents generated as an energetic particle passes through circuit elements (the radiation effects on electronics are fully explained in the next chapter). This type of effect is the main problem that needs to be addressed by the space community.

In conclusion, the space environment has a very wide range of radiation levels depending on the type of space mission. The electronics in each mission will endure different doses of radiation introduced by various fluxes of particles.

1.2 The ground level

The radiation effects on VLSI circuits at ground level were first reported by T. May and M. Woods [May78]. They discovered that errors in RAM chips due to upsets were caused by the alpha particles released by the contaminants within the chip packaging material. Chip vendors managed to find some specific solutions to reduce the alpha particles from the packing material to tolerable levels, mainly by reducing the alpha particle flux emitted by packaging and processing materials [Has92].

On the other hand, cosmic rays also exists on the ground, even if their intensity and energy are reduced compared to those of in the space. The secondary particles produced by cosmic rays are primarily neutrons. The others include protons and pions. The atmospheric neutrons are believed to be the major cause of the upsets occurring in VLSI circuits [Eng96, Zie96]. The neutron environment at ground level can be defined in terms of the models for the atmospheric neutron flux at higher altitudes which are mainly based on neutrons in the energy range of greater than 1 MeV and less than 10 MeV. It is shown by a number of studies [Nak87, Hew78] that the shape of the energy spectrum of the atmospheric neutron flux does not change with altitude or latitude, even through its absolute magnitude does vary with location and altitude around the Earth. Some data [Nor93] shows that a 10-100 MeV flux of neutrons falls off approximately linearly with decreasing altitude. Very few measurements of the neutron spectrum at ground level have been made. However, one set of most recent terrestrial spectral measurements [Eng96] shows that the ground spectrum is roughly 1/300 of that at 40,000 ft. An upset rate in the range of $1\text{-}2\times10^{-12}$ upset/bit-hour was shown to be representative of the rate that most SRAMs and DRAMs in actual field applications are experiencing. Some solutions have been introduced to reduce the impact due to the upsets caused by the neutrons. These include: improving the reliability of large computer system; applying error mitigation techniques to RAMs used in biomedical, commercial, and industrial products, etc.

1.3 The nuclear reactor environment

Three levels of radiation severity need to be considered for nuclear fission power plants: within the reactor core and cavity, in the containment, and in the containment under accident conditions [Lam83].

The major radiation sources in the reactor environment are neutrons and gamma rays (Kak86). The most important environment for equipment and components is 'in containment' and, while the gamma dose rate and neutron flux are moderate, the requirement for 40 years of operating life results in significant accumulated levels. Safety-critical equipment is required to operate at the end of a specified lifetime. Such equipment must also operate during and after a radioactive accident. Other stress factors must be taken into account in conjunction with radiation effects in order to arrive at a true estimate of the life expectancy and to define adequate qualification tests.

1.4 The radiation processing environment

Radiation processing is a branch of radiation technology, that involves the deliberate introduction of radiation damage into materials for beneficial purposes [Hol93]. The aspect of radiation processing which has caught the attention of the public in recent years concerns the irradiation of food products in order to eradicate harmful organisms and extend shelf-time. This is a small part of what is now becoming a major application in industry. Examples include the following:

- Modern consumer-oriented society generates a large amount of waste, and radiation processing is a potential solution for many of the problems involved in waste treatment and the cleansing of water supplies [Wal00].

- Radiation processing is used in the medical field for the sterilization of a number of products such as dressings, hypodermic needles, and catheters [Tur02].

- Industrial applications are increasing, particularly in the field of materials modification. The polymer industry uses radiation for the cross-linking of polymers to produce durable insulation for wires and cables, particularly for submarine use [Cam88]. Current investigations center around polymer grafting, with particular reference to the controlled delivery of drugs.

- The semiconductor industry is beginning to use radiation processing for the modification of starting materials, particularly silicon [Bel99].

- Many developing nations benefit from radiation processing. The economy of such nations frequently depends on a single perishable crop. Radiation processing is used to delay ripening and extend the period during which the crops may be brought to the market-place.

A wide range of radiation sources is used in the processing industry, such as gamma sources, electron accelerators, etc.

1.5 The weapons environment

A nuclear weapon based on fission is constructed with a configuration of fissionable material slightly below the critical point. A nuclear detonation is triggered when the configuration is made supercritical. This may be achieved either by driving two pieces of subcritical material together or by imploding a hallow spherical shell of material.

The energy associated with a nuclear weapon requires a special classification scheme. Nuclear yields are expressed in equivalent kilotons (kt) or megatons (Mt) of TNT explosive. One kiloton of TNT generates 10^{12} cal, which should be compared with the requirement of only 56 g of U-235 to release the same amount of energy [Mes86]. In less than 1 μs the detonation energy of a weapon escapes into an air mass many hundreds of times larger than the mass of the device itself.

The energy from the weapon is transferred by four mechanisms: thermal (fire ball), blast, nuclear radiation, and electromagnetic pulse (EMP).

The thermal and blast components are independent of the weapon construction; the radiation and the EMP component are determined by the weapon construction and materials and are independent of the external environment. The energy partition of a typical weapon detonated in the atmosphere is [Mes86]:

▪ Blast/shock	50 per cent
▪ Thermal radiation	35 per cent
▪ Delayed nuclear radiation	10 per cent
▪ Prompt nuclear radiation	5 per cent

The time division between prompt and delayed radiation is taken as 1 minute [Mes86].

The radiation consists of neutrons, X-rays, gamma rays, alpha particles, electrons and secondary particles. Some 90 percent of the neutrons generated by the fission-fusion reactions are absorbed within the bomb case. The neutron fluence is roughly proportional to yield.

The gamma rays originate from two principal sources:

- Prompt gammas generated in the first few milliseconds which come from a nucleus excited by capturing a neutron and then falling back to its ground state;
- Delayed gammas generated by the decay of radioactive fission fragments.

The gamma spectrum extends to 12 MeV with most of the fluence in the range up to 0.75 MeV. As with neutrons, the gammas undergo geometrical attenuation as well as exponential attenuation in materials [Hol93]. The gamma dose can be enhanced by the lowered density of the air during the blast.

1.6 High-energy physics accelerators

Current high-energy physics research is carried out with beams of electrons or protons having very high energies, often operated so that the two beams collide and produce short-lived particles of interest in determining subatomic structure. For example, the Large Hadron Collider (LHC) under construction at CERN in Geneva is a circular accelerator and consists of two adjacent 26.7 km rings in which two proton beams run in opposite directions [ATL]. The proton beams will collide at four points along the circumference at a centre of mass energy of 14 TeV. Many magnets and RF power sources are used to guide and accelerate the beam, and the target areas are surrounded by very large arrays of radiation detectors of the most advanced type, including high-speed, ultra-sensitive electronic detection circuitry.

At high luminosity the proton-proton collisions at the LHC will produce an extremely hostile radiation environment. Many simulations have been performed in order to obtain realistic expectations. The total dose contribution is mainly due to the primary flux of particles coming from the interaction region. The secondary radiation that escapes from the accelerator tube consists mainly of photons and neutrons of high energy. The dose rates are of the order of 10^5 Gy(SiO_2) per year [LHC]. The consequences for some parts and materials to withstand 10^6 Gy(SiO_2) opens up a new range of requirements generally higher than those needed in space radiation or the military environments.

Chapter 2 Introduction to Radiation Effects on MOS Devices and ICs

The interaction of radiation with matter is a very broad and complex topic. In this chapter, the basic mechanisms of the radiation effects on MOS devices are described, with the aim of explaining the important aspects which are essential for a physical comprehension of the degradation observed in MOS devices and circuits when they are irradiated. In section 2.1, the interaction between particles and matter in radiation environment is explained. Total dose effects in the MOSFET materials are listed in section 2.2 and the consequence degradation of electrical parameters are presented in section 2.3. The single-event effects are described in section 2.4.

2.1 Interactions between radiation particles and matter

Particles can be divided into two groups for simplicity: charged particles and neutral particles. The principal characteristic of charged particles is that they interact mainly through Coulomb interactions with the electronic clouds of the target atoms. The charged particles of interest are protons, heavy ions, pions and electrons. The uncharged particles are mainly neutrons and photons.

Protons give origin to the following phenomena:

- Coulomb interaction, which can induce ionization or atomic excitation (the latter for protons energy less than 100 keV),
- Collisions with the nuclei, which can cause their excitation or displacement,
- Nuclear reactions, which can occur for protons energies higher than about 10 MeV.

Unlike protons, many of which undergo collisions with nuclei and thereby deposit little energy, pions can be completely absorbed by a nucleus, depositing their entire rest mess and energy to the struck nucleus [Gel97]. Such a reaction results in a highly excited nucleus which deexcites by emitting neutrons and charged particles, including alpha particles. Heavy ions give origin, qualitatively, to a phenomena similar to those induced by protons.

Electrons, which can be present in the radiation environment or be produced by interaction of other particles with the material, can interact in two different manners, namely:

- Coulomb interaction, which can induce, as in the case of protons, ionization or atomic excitation,
- Scattering with the nuclei, which can cause physical displacement of the nuclei if the energy of the incoming electron is high enough and if enough energy is transferred to the nucleus.

Neutrons and photons differ from the charged particles because they do not experience the Coulomb force. According to their energy level, neutrons are divided into slow (energy less than 1 eV), intermediate and fast (energy greater than 100 keV), and give origin to three different phenomena of interaction with the atomic nuclei:

- Nuclear reactions: the incident neutron is absorbed by the nucleus, which afterwards emits other particles (protons, alpha particles, gamma rays). It is possible that nuclear fission can occur accompanied by the release of further radiation.
- Elastic collisions: the incident neutron collides with the nucleus and continues its path. If the energy given to the nucleus is sufficient, displacement of the nucleus can occur and the displaced nucleus can in turn cause ionization or further nuclear displacement.
- Inelastic collisions: the phenomenon is similar to the previous one, but in addition there is excitation of the nucleus, which afterwards decays, emitting gamma rays. The relative probability of these phenomena depends strongly on the neutron energy.

Slow neutrons give origin mainly to nuclear reactions or elastic collisions, and fast neutrons mainly to elastic collisions. For very high energies the inelastic collisions dominate [Hol93].

Photons interact with matter in the three different ways described below:

- The photoelectric effect, in which the incident photon ionizes the target atom and is completely absorbed. In addition, as the photoelectric electron is emitted, an electron in an outer orbit of the atom will fall into the spot vacated by the photoelectron, causing a low energy photoelectric photon to be emitted.
- The compton effect, in which an electron of the target atom is set free and a photon is emitted. The energy of the incident photon is divided between the two products of the interaction.
- Creation of electron-positron pairs. The incident photon is completely annihilated. This phenomenon never happens for energies of the incident photon less than 1 MeV. This value increases with decreasing atomic mass.

The probability of these three effects changes with the energy and also strongly depends on the atomic number of the target. The photons used in the radiation test of this work were X-rays with maximum energy of 320 keV.

The radiation effects of both charged and neutral particles on matter can be grouped into two classes: ionization effects and nuclear displacement. These phenomena may be caused directly by the incident particle or from secondary particles produced by it, and represent the overwhelming majority of the events which happen in the irradiated matter.

Ionizing radiation may be defined as charged particles that possess enough energy to break atomic bonds in the absorbing material, thus creating electron-hole pairs. The number of pairs created is proportional to the energy deposited in the material, which is the total absorbed dose. These charged particles may include protons, electrons and atomic ions with energies greater than the material band gap. Ionizing radiation can cause two primary effects in microelectronics: total ionizing dose effects (TID) and single-event effects (SEE). Total ionizing dose effects are caused by the accumulation of ionization over a period of time, which eventually leads to performance degradation and/or functional failure in microelectronics. Single-event effects refer to ionizing effects due to a single high-energy particle as it strikes the sensitive nodes (or sensitive volume) within the electronic device. It is primarily the result of currents generated as an energetic particle passes through circuit elements.

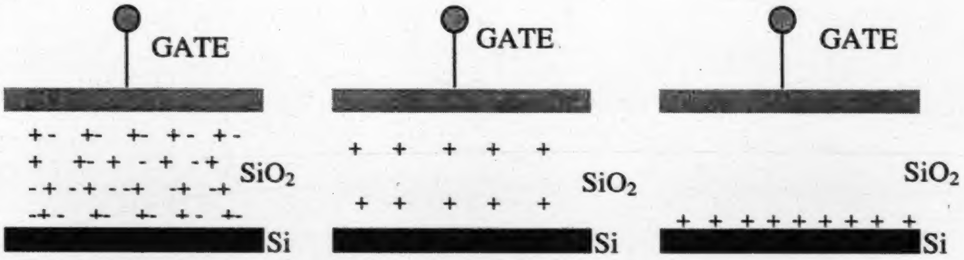
Atomic displacement in a lattice causes a neighboring interstitial atom and vacancy, which are called a Frenkel pair. In silicon dioxide at room temperature, 90 per cent of the pairs recombine within a minute after the end of irradiation [Hol93]. A main effect of the atomic displacement is the reduction of the lifetime of the minority carriers in the bulk, as the recombination rate of minority carries is changed by atomic displacement [Sro03]. CMOS transistors are almost entirely insensitive to displacement damage because their conduction is based on the flow of majority carriers immediately below the SiO_2-Si interface, a region that does not extend deep into the silicon bulk. To study displacement damage, neutrons sources are generally used.

2.2 Total dose effects

In this section, two sources that cause total ionizing dose effects are introduced: charge trapping in the silicon dioxide and at the Si-SiO_2 interface.

2.2.1 Charge trapping in silicon dioxide

MOS transistors are sensitive to ionization [Hol93]. The silicon dioxide is the sensitive part to the ionizing radiation as it traps charge induced by irradiation, which is shown in Figure 2.1. As ionizing particles pass through a MOS device, electron/hole pairs are generated (shown in Figure 2.1A). In the gate and the substrate the pairs quickly drift away because of the low resistance. On the other hand, electrons and holes have different behaviors in the oxide, which is an insulator. A fraction of the electron-hole pairs recombine immediately after being created. Mobile electrons move quickly through the oxide, but holes have a very low effective mobility in the oxides and are trapped in the gate oxide and field oxide (shown in Figure 2.1B). If the gate has a positive voltage, the holes move towards the SiO_2-Si interface. Close to the interface, but still in the oxide, some of the holes may be trapped, building a fixed positive charge in the oxide (shown in Figure 2.1C).



(A): Ionizing burst.

(B): After recombination and electron transport.

(C): After hole transport.

Figure 2.1: Illustration of charge trapping in the gate oxide of a NMOS transistor.

When the radiation-induced holes have migrated across the oxide, they can be trapped close to the SiO_2-Si interface. This phenomenon generally dominates over other radiation-induced phenomena, such as for example the trapping of electrons in silicon dioxide [Hug81]. As will be seen later, the trapping of holes in the oxide gives origin to a negative threshold voltage shift ΔV_{ox} which is not sensitive to the surface potential in the silicon and which can stay for a period of time varying from milliseconds to years. The amount of trapped charge is proportional to the number of defects in the silicon dioxide. For this reason one of the important steps for the fabrication of radiation-hardened technologies is to improve and control the gate oxide quality.

These trapped holes give rise to a threshold voltage shift, ΔV_{ox}, given by [Mul86 (p.401)]:

$$\Delta V_{ox} = -\frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{t_{ox}} \rho(x) dx, \tag{2.1}$$

where q is the electron charge, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the oxide capacitance, ε_{ox} is the dielectric constant of SiO_2 and t_{ox} is the thickness of the oxide, $\rho(x)$ is the spatial distribution of the oxide charge density, x is the distance along the spatial distribution.

Trapped holes can be removed (or neutralized by compensating electron trapping) either by thermal annealing or by the tunneling of electrons from the silicon substrate (or gate). Complete thermal-annealing often requires temperatures of up to 300°C or so [Dre98]. The distribution of energies inside the SiO_2 band gap for the trapped holes is quite similar for thermally-grown oxides fabricated by a wide variety of process (dry, wet, soft, hard, etc.). The shallower the trap level, the lower the temperature required to annihilate the trap (lower thermal activation energy).

Tunnel annealing can be used to explain the roughly linear with logarithmic time dependence often observed for the removal of trapped holes at moderate temperatures. This type of annealing can only affect those holes trapped within approximately 4-5 nm of the substrate or gate electrode because of the rapid decrease in tunneling probability with distance. However, this also means that significant neutralization of the trapped holes could occur via tunnel annealing in a relatively short time interval, for thin oxide (less than 10 nm).

2.2.2 Charge trapping at the SiO_2-Si interface

Another effect of radiation on CMOS devices is the increase by several orders of magnitude of the trapped hole density at the SiO_2-Si interface. This phenomenon has been studied for many years and several models have been introduced. Experiments indicate that both for NMOS and PMOS transistors the threshold voltage increases (ΔV_{it}, in absolute value) after irradiation due to the creation of new interface traps. It is strongly dependent on the processing steps of MOS devices, and there is generally no significant annealing of the generated traps at room temperature.

2.3 Radiation effects on the electrical parameters of a MOS transistor

In this section, the consequent degradation of electrical parameters caused by radiation effects is discussed. To be specific, these parameters are threshold voltage, subthreshold slope, leakage current, mobility, transconductance and noise.

2.3.1 Threshold voltage shift

The threshold voltage of a MOS transistor changes when the device is irradiated. This change has two contributions, the threshold voltage shift introduced by trapped charge in gate oxide (ΔV_{ox}) and by trapped charge at SiO_2-Si interface (ΔV_{it}).

In a NMOS transistor, the trapped positive charge causes a negative shift in the threshold voltage. This is shown in Equation 2.1. This can easily be understood qualitatively: for an NMOS transistor, for example, the positive charge trapped in the oxide repels the holes and attract electrons in the channel. This means that to re-create the same inversion condition one will need to apply a less positive potential to the gate. For a PMOS transistor, the opposite is the case.

The increasing trapped charge at the interface is a relatively slower phenomenon than the build-up of positive charge in the oxide. For this reason, V_{it} can change later than V_{ox}. This can also explain why the threshold voltage shift for NMOS transistors as a function of the total dose or the annealing time can be negative at the beginning and become positive at a later time (this effect is known as rebound). The slower temporal evolution of the radiation-induced interface states also plays an important role in the annealing of the irradiated circuits since this will decrease V_{ox} but will probably increase V_{it} both for NMOS and for PMOS transistors, affecting in this way the bias conditions of the circuit.

The measured threshold voltage shift ΔV_T is the sum of the two previously described contributions ΔV_{ox} and ΔV_{it}. To understand the behavior of both the trapped oxide charge and the interface traps it is interesting to separate the measured threshold voltage shift into two contributions. There are several ways of doing this [Doy93, Var91, Gro84, Bru69]. Our preference, also due to its simplicity, is the method described by McWorther and Winokur [Mcw86], based on the variation of subthreshold slope before and after irradiation.

The ΔV_{it} can be calculated from the subthreshold slope measurement [Mcw86],

$$\Delta V_{it} = \frac{\Delta Q_{it}}{C_{ox}} = \frac{q\Delta D_{it}\phi_B}{C_{ox}} = \Delta S \cdot \frac{q\phi_B}{\ln(10)K_B T} \; , \tag{2.2}$$

where ΔD_{it} is the variation of the interface state density, expressed in $V^{-1}cm^{-2}$. ϕ_B is the bulk potential. S and ϕ_B can be calculated by the following equations [Ane99a],

$$S = \ln(10)\frac{K_B T}{q}\left(1 + \frac{C_d + C_{it}}{C_{ox}}\right), \tag{2.3}$$

$$\phi_B = \frac{(E_i - E_F)}{q} = \frac{K_B T}{q} \cdot \ln\left(\frac{N_D}{n_i}\right). \tag{2.4}$$

S is subthreshold swing, which is determined by the unit area capacitance of the oxide (C_{ox}), interface trap capacitance (C_{it}) and depletion-layer capacitance (C_d). Typical values of S lie in the range of 70-100 mV/decade. From the Equation 2.3, it is shown that S is rather insensitive to device parameters, except for a slight dependence on bulk doping concentration through C_d and C_{it}. ΔS is the variation of the subthreshold swing. N_D is the doping concentration and n_i is the silicon intrinsic carrier concentration, that is equal to $1.45 \times 10^{10} cm^{-3}$ at 300°K.

Having measured ΔS and ΔV_T one is then able to calculate the threshold voltage shift given by the interface trapped charges ΔV_{it}, and also ΔV_{ox}. This is very useful when one wants to have information on the quality of the oxide and of the oxide-silicon interface, and also if one wants to study the annealing of the holes trapped in the oxide and of the interface states.

2.3.2 Change of leakage current: subthreshold and parasitic currents

The "off-state" current in a NMOS transistor is defined as the current which flows from drain to source when the gate to drain voltage (V_{gs}) is zero, and is also called "subthreshold leakage current" or simply "leakage current". Leakage current changes as subthreshold and parasitic currents change when an MOS transistor is irradiated.

The change in the subthreshold current has two components. The first one is the change of the threshold voltage. The second is the radiation-induced decrease of the subthreshold slope. For NMOS transistors, its leakage current increases if the threshold voltage shift is negative.

In addition to the transistors drawn in Figure 2.2, parasitic CMOS transistors can be generated during irradiation [Gai95]. In the past, local oxidation of silicon (LOCOS) has often been adopted for transistor isolation. Two parasitic paths are generated under the region called "bird's beak" or further away from the device, underneath the thick field oxide. In recent years, many commercial CMOS IC suppliers have replaced their LOCOS isolation with shallow-trench isolation (STI) for advanced submicron technologies to remove the lateral encroachment (no LOCOS bird's beak). However, the two parasitic paths still exist for STI, as illustrated in Figure 2.2. These parasitic elements cause leakage currents to flow around the edges of the drawn NMOS gate regions, from drain to source, between drain/source regions of adjacent NMOS transistors, and from n-channel drain/source regions to the n-well/n-substrate. This contribution to the total leakage current dominated over that one due to the subthreshold current in the deep submicron CMOS technologies [Sha98]. In chapter 6, the experiments done in this thesis also demonstrate this. The shift of subthreshold currents caused by irradiation is very limited, due to the very small value of $\Delta V_{T.}$

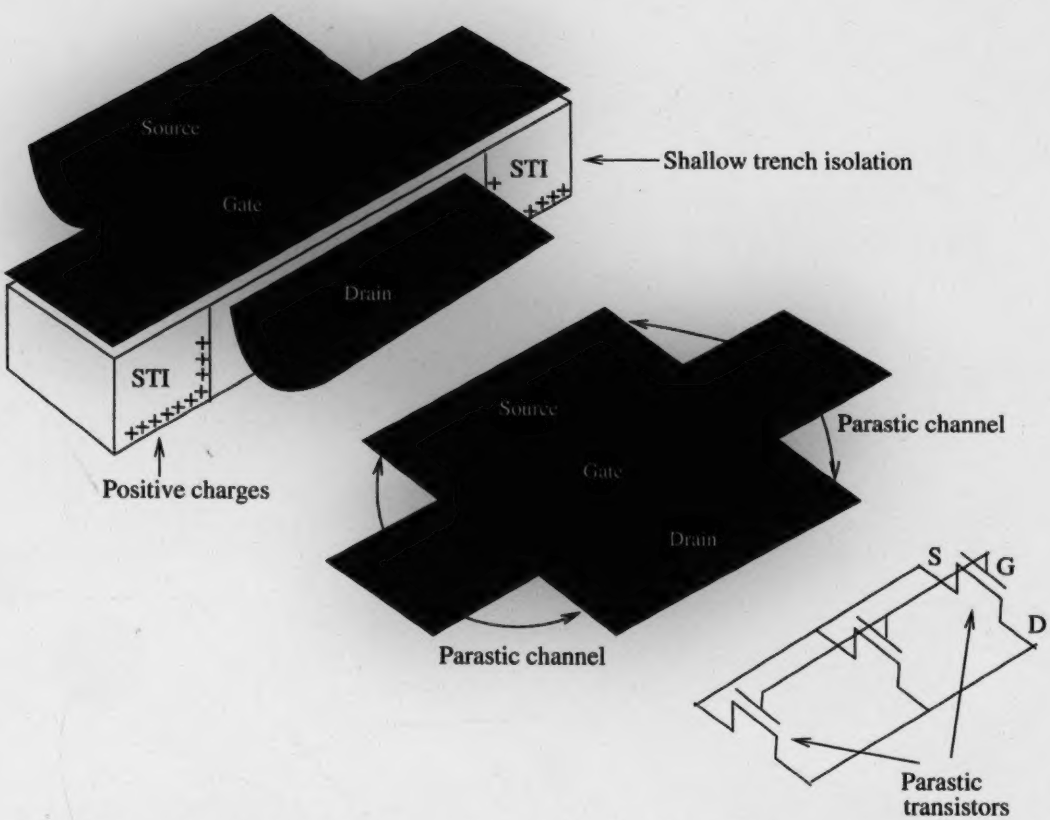


Figure 2.2: Illustration of the parasitic transistors that are in parallel to the main transistor and of the parasitic leakage paths in the shallow-trench isolation region or underneath the field oxide which connects the source and the drain.

2.3.3 Decrease of mobility and transconductance

Mobility degradation after irradiation is essentially related to the increase of the interface traps since the conduction in an MOS transistor is due to the carrier motion close to the SiO_2-Si interface. The mobility trend as a function of the increase of the traps can be expressed by the following empirical formula [Sex85],

$$\mu = \frac{\mu_0}{1+\alpha \cdot \Delta N_{it}}, \tag{2.5}$$

where μ_0 is the pre-irradiation mobility, ΔN_{it} is the increase of the interface traps and α is a parameter whose value depends on the technology. The degradation of the mobility gives origin to degradation in the transconductance. This decreases the driving capability of the device.

2.3.4 Noise increase

The noise characteristics of the MOSFET determine the lowest achievable circuit noise. After irradiation, one observes an increase in the white noise (the frequency-independent component) and the *1/f* (flicker) noise [Cha91]. The cutoff frequency (i.e. the frequency at which the two components are equal) moves towards higher values after irradiation. These effects are due to the increase in the concentrations of the interface traps and the traps in the oxide [Vit96, Tsi99, Cha91].

2.4 Single-event effects

The passage of a single particle through a CMOS device can create a high-density ionization track, which results in charge collection in a localized region of the circuit. The upsets caused by single-event effects (SEE) can be divided into two categories, soft upsets and hard upsets. The following gives a brief description of SEE. There are also some more in-depth analysis of SEE by J. Beaucour [Bea95].

2.4.1 Soft upsets

A soft upset occurs when a transient pulse or bit-flip in the device causes an upset detectable at the device output. Soft upsets are entirely device-specific, and are best categorized by their impact on the device.

2.4.1.1 Single-event upset

A single-event upset (SEU) [Die82] occurs when the charge transferred as a result of the generated short pulse of currents is of sufficient magnitude to alter the logic state of a sensitive node. A sensitive node is a node that can collect charge on it when hit by a particle. A single charged particle can traverse through a transistor's reverse-biased p-n junction and create an ionizing path along its line of trajectory. Figure 2.3, shows the effect of an alpha particle striking a node in an array of circuit nodes, with the dashed curve representing the expected charge collection through the diffusion mechanism. However, the electric field across the junction is distorted along the ionizing path (this is called funneling) [Mcl82], which increases the electric field's ability to attract the charge to one of the nodes. Taking the funneling phenomenon into consideration, more charge would be collected at the struck node and less at the surrounding nodes. If the charge collected at the node were within the indicated range, an upset would occur. The minimum charge, which must be deposited in a device to cause an upset, is called the critical charge.

An upset node may further cause the alteration of the contents of circuit memory elements or alter the operation of the circuit in such a way as to cause an upset in the logic function. In the case of a static RAM cell (SRAM), which is made of two inverters in which the output of each inverter is connected to the input of the other one, the sensitive nodes are the transistors' drains. This kind of problem is of special concern in digital circuits and can be eliminated by rewriting the information lost in the case of a memory or repeating the algorithm being executed in the case of a CPU. The number of soft upsets is normally specified in upsets/bit-day. If the upset rate is too high this can lead to a significative reduction in the circuit performance.

A SRAM stores information in a latch. For an SEU to occur, the induced perturbation must exceed the charge restoration capability of the cross-coupled inverter. By a similar argument, the cell can be hardened against SEU by protecting the charge at one inverter's gate. For CMOS SRAMs that have very low static power consumption, the critical charge provides a valid measure of SEU susceptibility. The duration of the charge collection from a SEU is short compared to the write time of the SRAM cell.

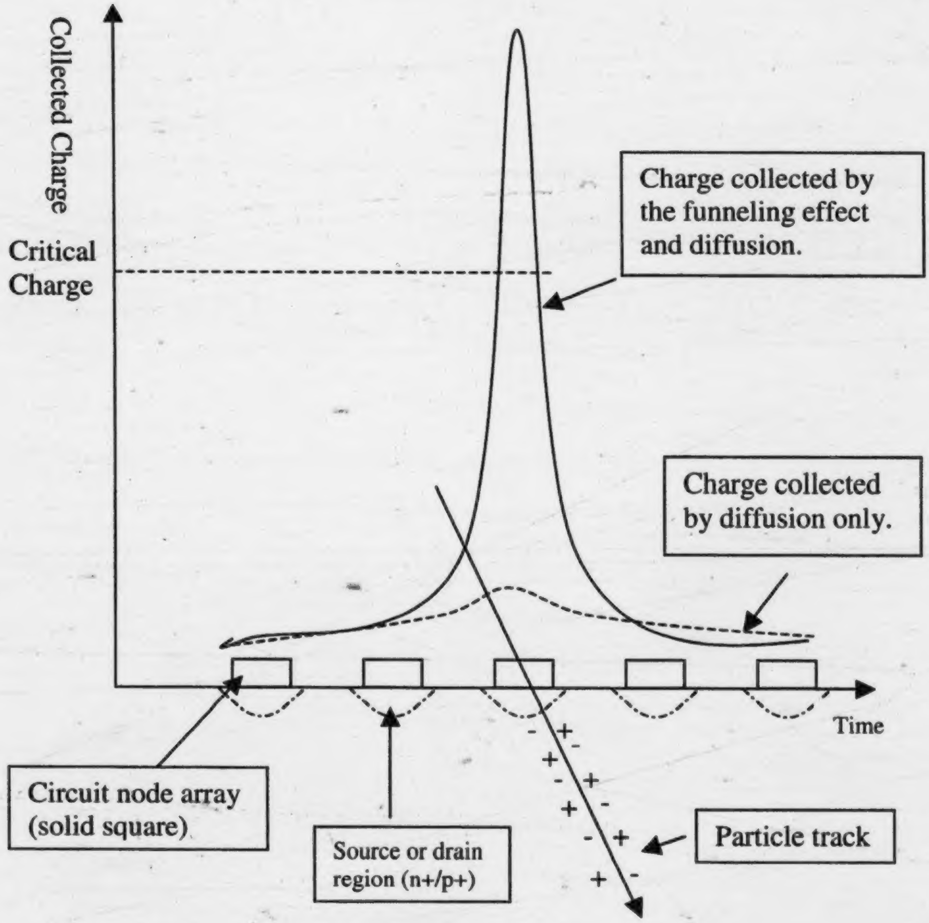

Collected Charge
Critical Charge
Charge collected by the funneling effect and diffusion.
Charge collected by diffusion only.
Time
Circuit node array (solid square)
Source or drain region (n+/p+)
Particle track

Figure 2.3: Illustration of charge collection profiles for a target node from the diffusion and combination of diffusion with funneling effects. The collected charge changes with time which is shown in the diagram. The circuit node array and particle track are shown in a cross-section diagram.

In general, SRAMs radiation-hardened for both total dose and SEU are preferred for critical space and high-energy physics applications.

2.4.1.2 Single-event functional interrupt

Single-event functional interrupt (SEFI) can be thought of as a special case of SEU. In complex memories, the memory cells and the peripheral circuits of a memory are connected to other circuits. If an energetic particle strikes one of these circuits, the upset could influence the functioning of the whole circuit.

2.4.1.3 Multiple-bit upset

Multiple-bit upset (MBU) is analogous to the SEU, but more than one node is affected at the same time. There are three different kinds of upsets: the first two are caused by a single particle, the third by two independent particles. In the first case a single particle strikes the integrated circuit at nearly a right angle to the surface, crossing in this way the sensitive volume of more adjacent devices at the same time. In the second case the particle strikes the node almost perpendicularly to the surface but deposits enough energy to be able to change the information contained in more than one sensitive node. As the feature size is reduced, MBU will be more and more common in VLSI circuits [Joh99]. In the third case two particles hit two nodes simultaneously, modifying their states.

2.4.2 Hard upsets

Hard upsets can be physically destructive to the device and cause permanent functional errors.

2.4.2.1 Single-event latch-up

For CMOS circuits containing both NMOS and PMOS transistors on a silicon substrate, parasitic bipolar p-n-p-n devices exist and form a silicon-controlled rectifier (SCR) structure, which under normal conditions is in its “off” (i.e. high-impedance) state. If a radiation-induced current produces sufficient bias to turn on one of the parasitic base-emitter junctions, the SCR can be triggered, producing a low-impedance path between the power supply and ground rails. If the product of the effective current gains of the parasitic p-n-p and n-p-n devices is greater than unity, then a self-sustaining SCR high current mode is triggered. This condition is known as single-event latch-up (SEL) [Joh96, Mul86 (p. 458)]. The SEL phenomenon is similar to the electro-static discharge induced latch-up, which is protected against in typical CMOS I/O structures. However in an ionizing radiation environment, a particle can strike anywhere in the circuit so merely protecting the I/O circuitry is not sufficient. SEL is a potentially destructive condition. During a destructive SEL, the device current exceeds the maximum specified for the device. Unless the power is removed, the device will eventually be destroyed.

2.4.2.2 Single hard error

If a particle crosses the gate oxide layer of an MOS transistor, it may deposit a sufficiently large total dose to induce a permanent threshold voltage shift, which results in the functional failure of the device [Duf92]. This phenomenon is called single hard error (SHE). SHE causes a permanent change to the operation of the device. A common example would be a stuck bit in a memory device. Like SEUs, this is also device dependent. For example, in a DRAM cell, the subthreshold current of the pass transistors can become high enough to conduct the charge on the storage capacitor to the word line all the time and no information can be stored in the cell.

2.4.2.3 Single-event gate rupture

Single-event gate rupture (SEGR) [All94, Whe94] is an irreversible event that consists of the destruction of the gate oxide by an ionizing particle. This problem is especially important in the situation where there is a high electric field on the gate oxide, as for example during the writing or erasing phase of EEPROM (Electrically Erasable Programmable Read-only Memory) or in power MOSFET devices.

2.4.2.4 Single-event burn-out

Single-event burn-out (SEBO) [Hoh87] can occur in power MOSFET's and bipolar transistors since these devices contain a parasitic bipolar transistor. In some biasing conditions it is possible that an ionizing particle turns on the bipolar transistor, and if this is able to conduct enough current, the local power can be high enough to melt and destroy the entire transistor.

2.5 Summary

There are three primary types of radiation effects:

- Total dose effects result from the interaction of ionizing radiation with silicon oxide, generating charge which change device properties. These effects depend upon the total ionizing energy absorbed in the material (the total dose).
- Single-event effects result from the interaction of a single energetic particle passing through a device. Historically these effects have been associated with the high density charge track created by the particle.
- Displacement damage effects result from the displacement or dislodging of atoms from their normal site in a crystal lattice or material structure due to the nuclear interaction of energetic particles. These interactions create defect sites in the material. MOSFETs are not sensitive to this type of effects, as the MOSFET is using majority carriers instead of minority ones, which are affected by displacement damage effects.

Chapter 3 Deep Submicron CMOS Technologies for Radiation Applications

CMOS technologies are scaling down rapidly in physical size. For the current technologies, the minimum feature size is well below a micrometer. Normally, the technologies with feature size less than 0.5 μm are referred to as deep submicron technologies. The first part of this chapter reviews the scaling laws of CMOS technologies. The scaling of CMOS technologies brings some beneficial and detrimental effects to integrated circuits in a radiation environment.

3.1 Technology scaling

Since the production of single planar transistor in 1959 the density for ICs has grown exponentially, as was foreseen in 1965 by Gordon E. Moore [Moo65]. A practical example of how Moore's law works is seen from the early seventies up to now in Figure 3.1. This scaling process which happened in the past is expected to continue in the near future. Detailed projections on future trends can be found in [SIA99]. The most interesting scaling features are reported in Figure 3.2. Projections show that in the year 2014, CMOS transistors will have a 35-nm gate length and a supply voltage of 0.3 V. This evolution will influence the intrinsic radiation tolerance of commercial CMOS technologies. The principles used when a CMOS process is scaled down [Tsi99 (pp.290-296)] are reviewed below.

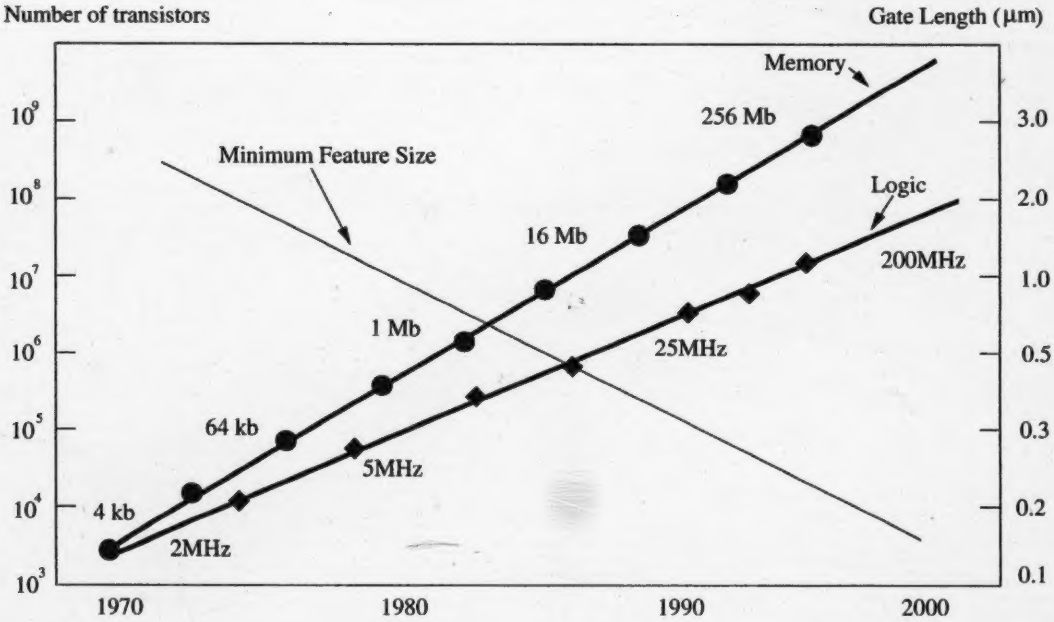


Figure 3.1: The plot shows how scaling density and speed vary with time (i.e. decreasing the minimum feature size). The data are taken from [Cit99]. The left side of the Y-axis indicates the number of transistors on a chip; the right side of the Y-axis is the minimum gate length of the transistors.

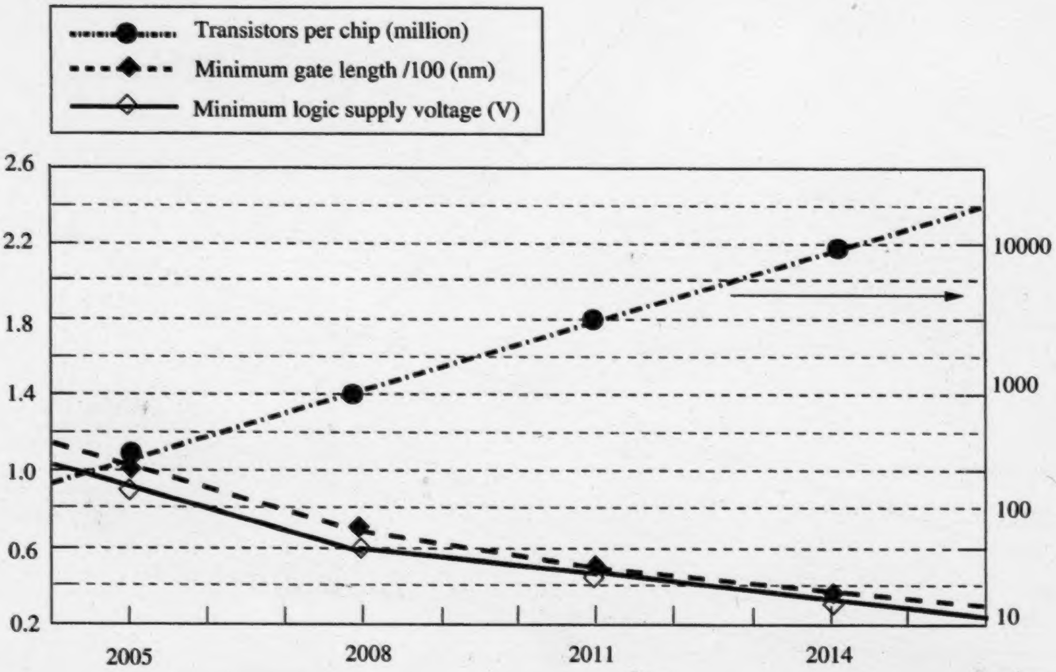


Figure 3.2: Technology trends foreseen for the next 10 years. The data are taken from [Ane99a]. The line with the round markers refers to the right axes (logarithmic scale), the others to the left axes (linear scale).

The aim of scaling is to reduce the device dimensions without introducing effects which degrade the operation of the device. Several scaling procedures have been proposed in the past [Den74, Yh79, Bre80, Cha80, Elm82, VLS82, Kin83, Rei83, Shi83b, Bac84, Pfi85, Cri99]. Some of these procedures and their associated problems are given below.

- **Constant field scaling procedure** [Den74, Dav95]. In this procedure, the device and its depletion region are a scaled down version of a large device. All the physical dimensions are divided by a factor. The voltages are also divided by the same factor. The electric field in the scaled devices is similar to those of the larger ones. In this way, it gives a real improvement in the performance without changing the electric field and the power dissipation per unit area. But it also presents some problems. The major problems are related to the scaling of the power supply voltage and to the fact that the weak inversion slope does not scale down properly, which means that the subthreshold current is higher than it is supposed to be. In practice, the threshold voltage cannot be scaled by the same factor, to avoid the very high off-state weak inversion currents.

- **Constant voltage scaling.** In this approach, the transistor's width, length and doping concentration are scaled as before, but the voltages do not change. In this way, power supply compatibility is preserved between different logic families. If the oxide thickness is also scaled by the same factor, then the electric field in the oxide would be too high, causing some serious problems. For this reason, the oxide thickness is scaled less drastically [Cha80].

The above two scaling methods are somewhat extreme. Some intermediate approaches have been proposed, such as quasi-constant scaling and generalized scaling [Bac84]. In quasi-constant scaling, the geometric dimensions and the substrate doping are scaled down as in the constant field scaling, but the voltages are scaled less drastically. But this creates a problem since the depletion region does not scale in the same way as the other geometrical dimensions. This problem is overcome in the generalized scaling where the doping concentration is scaled appropriately so as to have the right depletion region width.

3.2 Beneficial radiation effects of technology scaling

3.2.1 Total dose tolerance

The scaling of CMOS technology reduces the thickness of the gate oxide. This improves the radiation tolerance of the gate oxide since the effects due to the holes trapped in the oxide and to the radiation-induced interface states decrease as the square of the gate oxide thickness for oxides thicker than 10 nm, and even faster for thinner oxides [Jar99]. The thin gate oxide of a deep submicron CMOS transistor is intrinsically more radiation-tolerant than thicker oxides. The threshold voltage shift, the degradation of the mobility and the change in transconductance are very small even after doses of several hundred of kGy(SiO_2) [Jar99, Sno00]. Figure 3.3 shows the threshold voltage variation per 10 kGy (SiO_2) dose as a function of oxide thickness. This plot shows how scaling dramatically improved the intrinsic radiation tolerance of the gate oxides. The plot also shows that the improvement from the 0.7 μm technology to the 0.25 μm technology is almost of two orders of magnitude. This is mainly due to the hot carrier effect, which recombines the trapped charges in oxide and oxide-silicon interface within approximately 4-5 nm. The work done in this thesis (chapter 6) shows that the threshold voltage variation per dose is less than 5 mV/10 kGy(SiO_2) for the 0.18-μm CMOS technology.

Other non-radiation beneficial effects of scaling are general improvements in technology performance, such as speed, area, and power consumption.

3.2.2 Single-event latch-up

As introduced in the previous section, a latch-up failure involves a high current path between power and ground triggered by a parasitic regenerative structure. After the triggering process, external circuit conditions must allow the regenerative condition to be sustained. Scaling introduced some changes in the device structure which help in preventing SEL [Joh96]. These modifications include epitaxial layers, trench isolation and retrograde wells, which together with the reduction of the power supply voltage, help to reduce the risk that parasitic thyristors will be turned on by an ionizing particle.

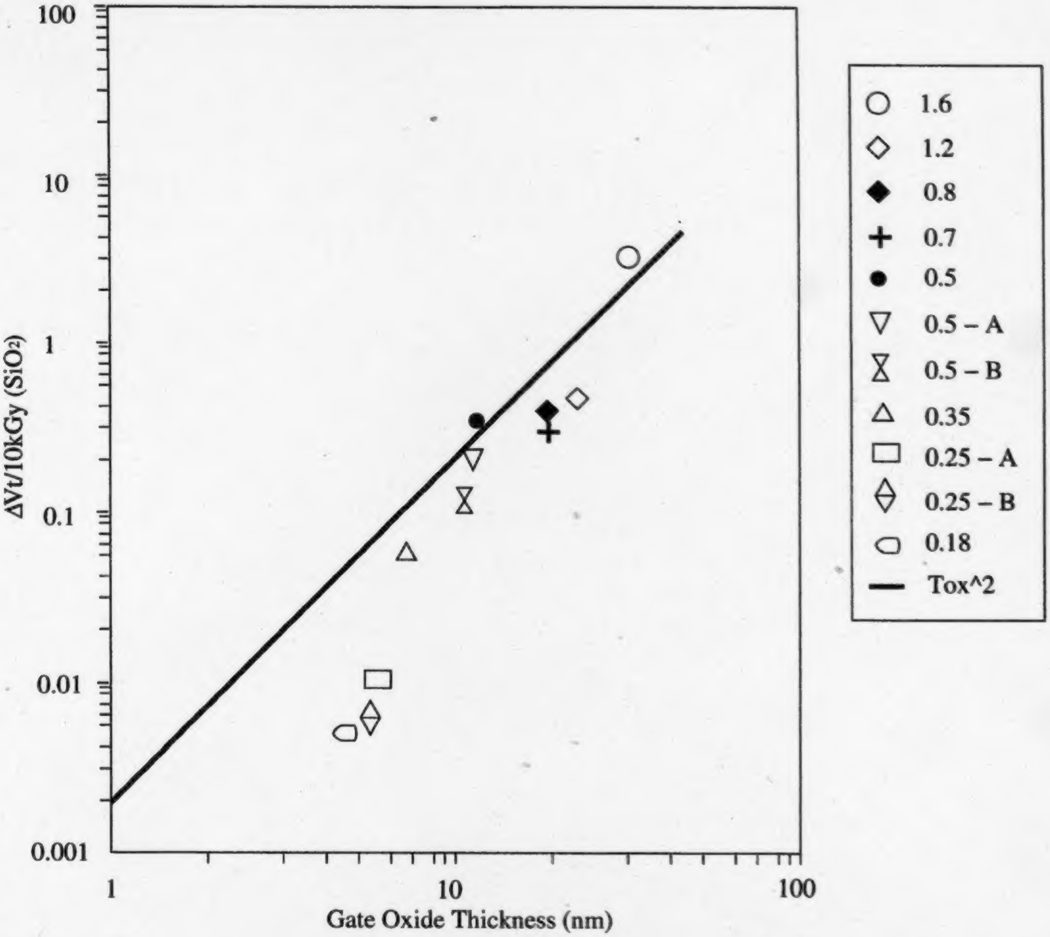


Figure 3.3: Threshold voltage variation per 10 kGy(SiO_2) dose as a function of the gate oxide thickness (T_{ox}). A and B in the legend indicate technologies from different manufactures. Some of the data are taken from [Ane99].

3.3 Detrimental radiation effects of technology scaling

Scaling also has some detrimental effects both on the radiation tolerance and on the circuit architectures. Deep submicron technologies are generally more sensitive to SEU than older technologies. The impact of SEU on the memories, because of their shrinking dimensions and increasing densities, has become a significant reliability concern [Joh98, Sex97]. As the devices are scaled down, the charge stored on the nodes decreases since both the capacitances and the power supply decrease, making it easier to upset a memory cell. This means that the critical charge to upset a logic state becomes smaller and smaller. Figure 3.4 shows a plot of SEU critical charge versus feature size for a broad range of technologies [Pet]. This curve shows a lack of dependence on the device technology, and seems to follow the L^2 scaling rule.

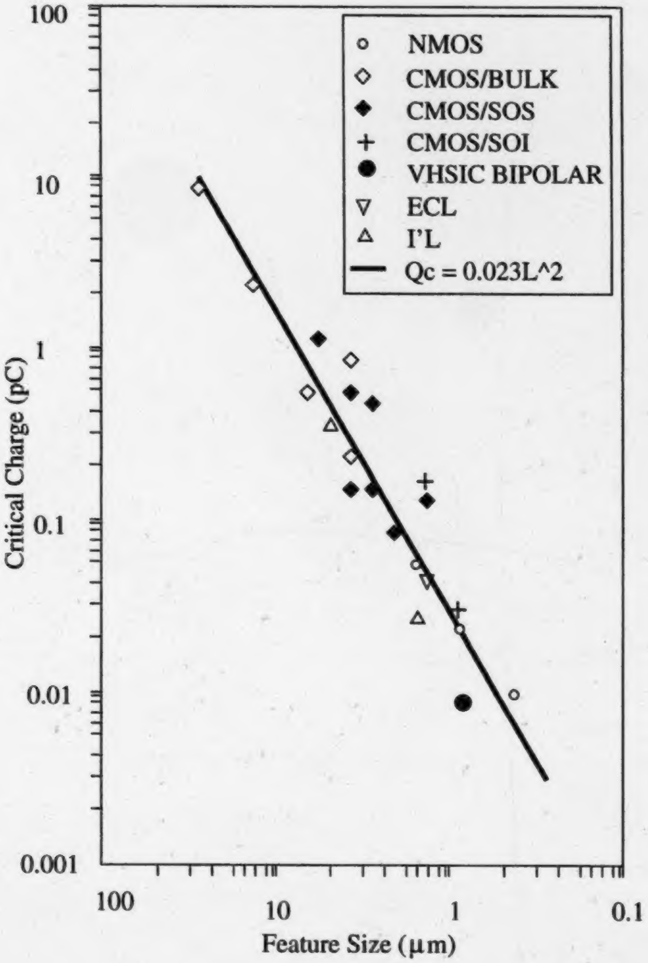


Figure 3.4: SEU critical charge versus feature size for various technologies. The data are taken from [Pet].

Chapter 4 Radiation-Hardening Techniques

The radiation hardness of circuits is influenced by a number of factors, both process- and design-related. CMOS is the preferred technology used in the fabrication of radiation-hardened circuits because of its lower static power and high noise margin features. In section 4.1, process-related hardening techniques are introduced. In section 4.2, layout-related hardening techniques are presented that aim to reduce the leakage current caused by total dose effects. In section 4.3, circuit and system-related hardening techniques are discussed, mainly to solve the single-event upset problem.

4.1 Process-related radiation-hardening techniques

Some of the process-related factors that affect the radiation response are substrate effects, gate oxidation, gate electrode effects, postpolysilicon processing, and field oxide hardening. Radiation-hardened CMOS processes have to take into account these factors. Except that, CMOS Silicon-On-Insulator (SOI)/Silicon-On-Sapphire (SOS) technologies utilize insulator isolation as opposed to junction isolation for bulk technologies and therefore also offer a substantial advantage in SEE characteristics. In general, process-related radiation-hardening techniques can provide immunity both to total dose effects and single-event effects. But as shown in Figure 4.1, there is typically a seven-year performance gap (more than two generations) that has been incurred for space-qualified microprocessors over the past decade compared with commercially available processors. This performance gap is anticipated to remain approximately constant in the near future [Lac00]. Some other concerns are cost and access to fabrication facilities.

There are vendors of radiation-hard CMOS electronics. However the number of available radiation-hard processes has decreased in the past decades, due to the reduction of the military market. The existing radiation-hard processes are normally several generations behind commercial technologies, which do not fit the low power and high-density requirements of the complex circuits to be used in LHC. Only a few of these vendors provide assistance and tools for custom circuits and most of their products are digital, which are aimed mainly at microprocessor applications for space and military communities. Therefore, two major issues have to be solved for high-energy physics community: access to radiation-hard technologies and the performance of the circuits in analog applications where low noise is essential.

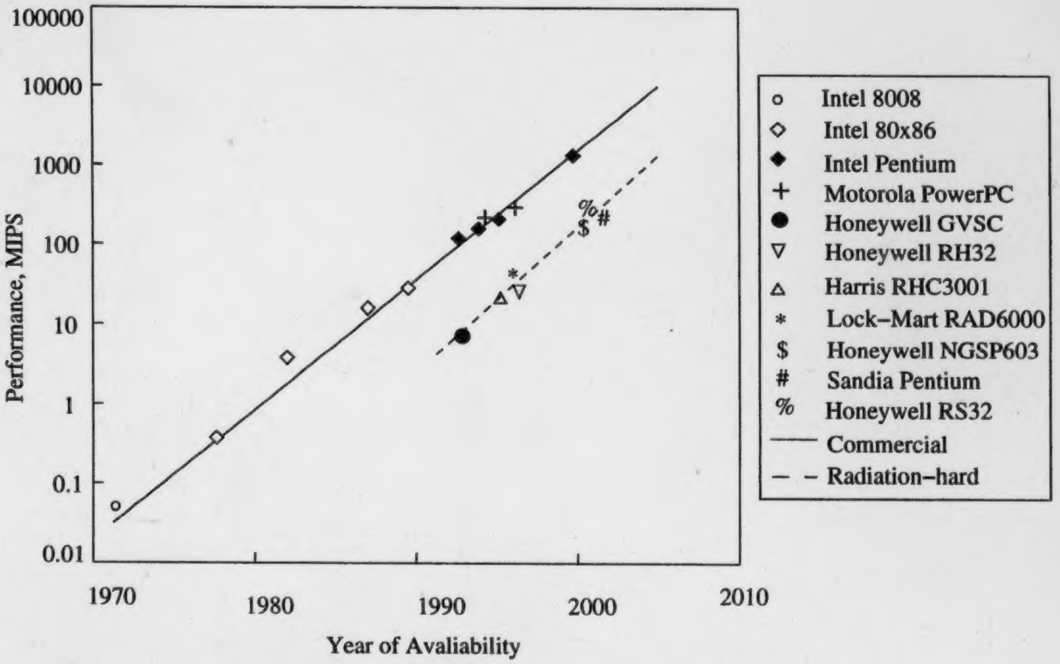


Figure 4.1: Microprocessor performance versus year of introduction for commercial and radiation-hard microprocessors. The data are taken from [Lac00].

4.2 Layout-related radiation-hardening techniques

Due to the disadvantages of radiation-hardened processes, other radiation hardening techniques have been introduced. Limiting the supply current to a device can save it from latch-up destruction, but requires a power down and reset cycle whenever a SEL occurs. Logic malfunctions due to SEUs can be detected and corrected through system-level redundancy and majority vote-checking schemes. However, this strategy can be quite costly and still leaves unanswered the classic question, “who checks the checker?”

In an attempt to reduce the costs and improve the circuit performance, the possibility of using a deep submicron commercial technology for application-specific integrated circuit (ASIC) design is becoming more and more attractive [Ane99]. Such an approach is based on the increased radiation tolerance of the gate oxide, which accompanies the shrinking of CMOS processes [Sak86]. It has been demonstrated that circuit and layout design techniques can make it possible to provide a high degree of SEL and SEU immunity using commercial CMOS processes [Ane97, Ane99].

The leakage currents introduced by parasitic NMOS transistors becomes the dominating factor compared to leakage currents introduced by gate oxide in deep submicron technologies. So the primary problem that has to be addressed is the irradiation-induced leakage current introduced by parasitic transistors inside the NMOS transistors. PMOS transistors are less susceptible to irradiation as the leakage currents of p-channel parasitic transistors become less and less significant after irradiation. The reason is that the threshold voltage of p-channel parasitic transistors increases after irradiation, which means that the leakage current decreases after irradiation. Figure 4.2 shows the problem in a standard NMOS transistor (Figure 4.2A) and three possible solutions [Hat85, Hat86]. Solution B (Figure 4.2B) consists of increasing the length of the parasitic devices. It is the least intrusive but also the least effective. With the solution C (Figure 4.2C) the limits of the thin oxide are defined with a mask (p+ diffusion in the figure) and inside this thin oxide region the transistor is defined. This solution permits keeping the transistor geometry very close to the one of the standard transistor, but it is not generally applicable in commercial processes since it violates some design rules which do not allow P+ diffusion immediately surround a n+ region). Moreover, for high enough total doses a parasitic path could still exist underneath the gate at the border of the thin oxide region. The solution D (Figure 4.2D) is the one adopted in this work as it is the safest from the radiation hardness point of view. In this case the parasitic path that connects the drain to the source is eliminated. The disadvantages in using this transistor layout are:

1. A larger area (less density),
2. Increase in the gate, source, drain capacitances,

3. Extra effort in modeling the width/length (*W/L*) ratio,
4. Lack of symmetry,
5. Limitations in the choice of the *W/L* ratio (see section 4.2).

Enclosed-gate transistors have been used in the early days of CMOS transistors [Din77a, Din77b] and their effectiveness in preventing leakage currents in irradiated integrated circuits is well known [Nap82, Ale96]. For our applications, they were used intensively in designing complex digital circuits. These use lead us to investigate in depth many issues useful for a designer, such as modeling of the effective *W/L* ratio, which will be treated in the next chapter.

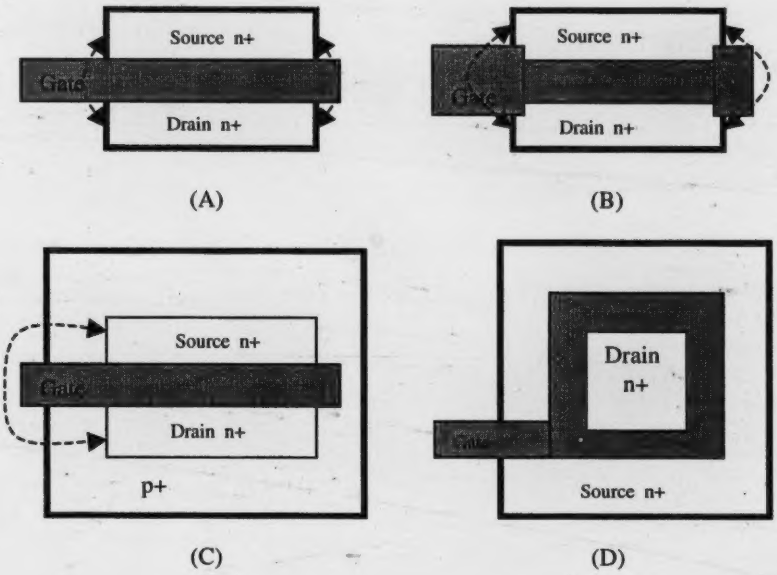


Figure 4.2: Layouts of a standard self-aligned NMOS transistor (A) and of three possible alternatives (B, C, and D) to inhibit the leakage paths shown in the standard transistor. The thin oxide areas, where there can be a creation of a radiation-induced parasitic path, are indicated with thick black lines. The leakage paths are represented with dashed lines.

The second problem that can be solved with a layout technique is the radiation-induced leakage current between different devices (Figure 4.3). The solution to this problem is to surround each NMOS device with a p+ guard ring, which cuts any possible radiation-induced parasitic path. This method has been verified to be very effective for total ionizing dose effects and single-event latch-up [Ane99]. The drawback is that this method is area consuming.

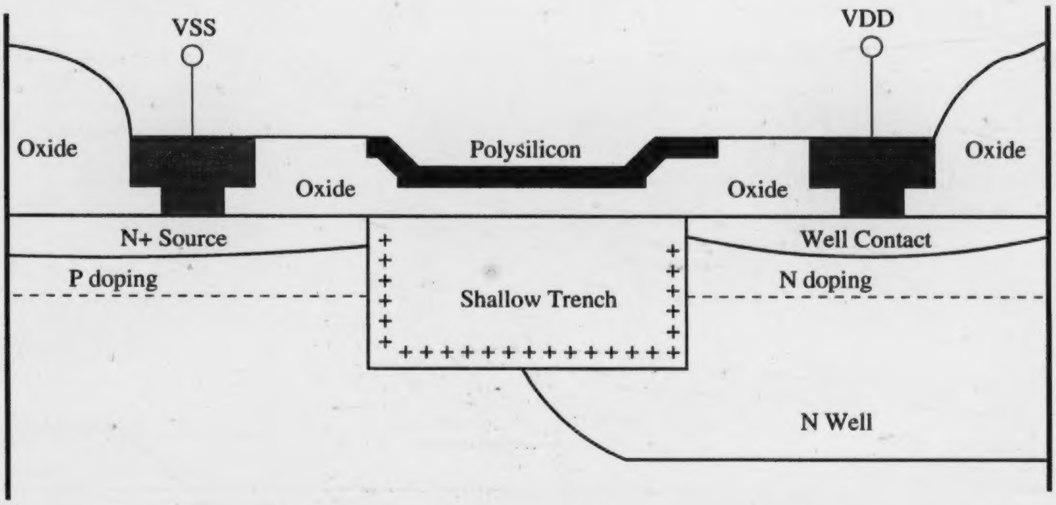


Figure 4.3: Illustration of a radiation-induced parasitic path in an n-well CMOS technology with shallow-trench isolation. The well of a PMOS transistor, connected to the power supply, is leaking toward the grounded source on an NMOS transistor. If a biased interconnection line (made of polysilicon in the case of the figure) passes over the thick oxide, it worsens the problem.

A third problem that can be addressed with layout techniques is single-event latch-up (SEL). The possible solutions are:

1. Increase the distance between the p+ diffusion in the well and the n+ in the substrate,
2. Increase as much as possible the number of substrate and well contacts, and put them as close as possible to the latch-up loop so that the resistances are minimized,

3. Put p+ guard rings around the NMOS transistors (this would be done anyway to solve the leakage problem) and n+ guard rings around the PMOS transistors. The p+ guard rings decrease the gain of the NPN parasitic bipolar transistor, introducing a strongly doped p+ region in the base and keeping the base firmly close to ground. The behavior of the n+ guard rings with the PNP parasitic bipolar is similar.

Figure 4.4 shows the layout of an inverter with a normal PMOS transistor and an NMOS ELT. The transistors are enclosed with guard rings. All of the rules explained previously are respected in the layout.

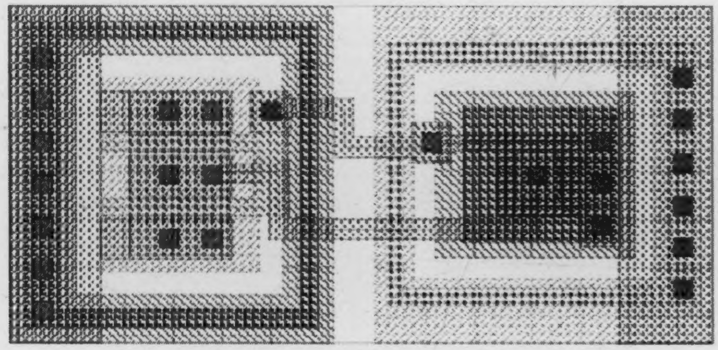


Figure 4.4: Layout of an inverter using the proposed radiation-tolerant layout approach in a CMOS technology. The n-well layer is not shown in the figure.

Hardening by layout can also reduce the sensitivity to SEU. This can be simply achieved by increasing the *W/L* ratio of the transistors, which increases the capacitance and the driving power, or adding additional capacitances to the most sensitive nodes.

4.3 Circuit and system-related radiation-hardening techniques

To harden a circuit for total dose several techniques can be applied. Modeling the radiation-induced variation of several transistor parameters, such as the transconductance and the threshold voltage as a function of the total dose, allows one to predict the drift of the circuit operating point, and therefore one can design the circuit in order to make it resistant enough to tolerate these drifts. For digital circuits, the synchronous mode of operation is better than the asynchronous, since synchronizing the logical states with a clock limits the sensitivity to transition time variations and to drifts in the electrical parameters.

SEE hardening can also be achieved with several methods. For SEU, static architectures are in general harder than dynamic architectures and further hardening can be achieved by modifying the critical charge or filtering the transitory effects generated by highly energetic particles. This second technique is shown in Figure 4.5. The fast disturbing effect of the striking particle is filtered with the two resistances, which slow down the circuit so that it does not have time to react, i.e. to flip. Resistive hardening [Wea87], on the other hand, seriously degrades the latch speed, especially at low temperatures (less than -10° C).

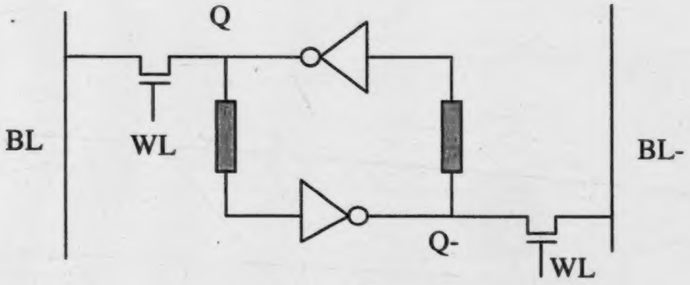


Figure 4.5: Schematic of a resistor-hardened SRAM cell.

Using special circuit architectures is another effective way to obtain SEU hardening (design hardening). The basic idea is to provide memory elements with an appropriate feedback devoted to restoring data when corrupted by a charged particle. Many design hardened memory elements have been proposed in the last ten years. An exhaustive explanation of the development of these memory elements can be found in [Bes94, Vel94]. The proposed solutions and their advantages and drawbacks will be briefly recalled here. A first approach consists of building a memory cell from gates taken from a SEU-immune CMOS logic family, such as the one proposed in [Can91]. This solution presents two main problems: a long recovery time after an upset and leakage current problems that could appear due to total ionizing dose effects. Nevertheless, a prototype implementing shift-registers built from master-slave flip-flops designed using this approach has been tested [Wis93] and shows excellent SEU immunity (no upsets were detected for particles with linear energy transfer (LET) up to 120 $MeVcm^2mg^{-1}$). A different design solution was presented in [Roc88]. Shift registers built with hardened latches designed using this solution showed its effectiveness (no upsets were detected for particles having LET up to 74 $MeVcm^2mg^{-1}$). An original memory cell design was presented by [Whi91] and an improved version followed one year later [Liu92]. Even though this cell has only two sensitive nodes, the test results presented in [Wis93] showed that this design solution was not SEU-immune. Two new SEU-tolerant memory cells were presented in 1994 [Vel94], which showed several advantages such as limited number of transistors, short recovery time and low static power consumption. Another new storage cell design was presented in [Cal96]. The cell is called Dual Interlocked storage Cell (DICE), and achieves upset immunity while avoiding the drawbacks of earlier solutions.

At the system level, several solutions for SEE hardening have been proposed [Lab96]. For SEU, a preliminary analysis of the system is necessary to estimate the upset rate in the sensitive circuits of the system and to evaluate how an upset in a given circuit will influence the functioning of the entire system. The weak point in the system can then be hardened by using techniques of Error Detection and Correction (EDAC) [Hen02]. These techniques add some bits to the normal digital "word" and, depending on the complexity of the correction system adopted, they can detect or correct single or multiple bit upsets. One way to deal with SEU at the system level is to use redundancy. Triplicating the hardware and applying a majority vote scheme is an example of redundancy [Sav98].

Chapter 5 Modeling of Enclosed-Gate Transistors

The MOSFET standard layout consists of a source and a drain separated by a channel *W* wide and *L* long. The enclosed-gate MOSFET is a transistor with the drain (or source) diffusion in the middle surrounded by the gate and the source (or drain) diffusion. The enclosed-gate MOSFET was originally used when MOSFET technology was first introduced to reduce the leakage current. With the advancement of MOS technologies, this layout technique gradually became unnecessary. It is now only used in some special cases, i.e. high temperature low power analog design. CERN started to systematically analyze and use enclosed-gate CMOS transistors in their high-energy physics projects in the late of 1990's [Cam99, Jar99, Sno00].

Modeling issues of ELTs, aimed at the design of radiation-tolerant ICs, are presented in this chapter. It is necessary to study the characteristics of enclosed-gate transistors and the standard layout transistors for the purpose of understanding the impact of the enclosed-gate transistors on digital and analog circuit design. The deep submicron MOSFET introduces complications for modeling [Fot97, BSIM3]. Here a first-order model for the effective aspect ratio is introduced for the enclosed-gate devices. The formula is then verified by experiment results. The output characteristics of the ELT are also studied.

5.1 *Aspect ratio calculation*

There is a wide range of possible shapes for ELTs: for example, circular, square, octagonal, and square with the corners cut at 45°. All of them could have different characteristics and need to be modeled separately. Information about modeling of a generic ELT can be found in [Gri82, Gir98, Gir00]. The shape shown in Figure 5.1, broken corner square, is adopted as it is compatible with the design rules of many deep submicron technologies. The corner size, *c* is kept small and constant to have as small an effect on the overall transistor as possible. *L* can be varied to make the current flow mainly in two orthogonal directions and ensures a better uniformity. Modeling of the aspect ratio is focused on this type of shape.

By decomposing the transistor into three parts, labeled T1, T2 and T3 in Figure 5.1, its total aspect ratio of *W/L* can be represented in a formula by three terms. The first part corresponds to the four linear edge transistors (T1); the second part corresponds to seven or eight angle corner transistors (T2) that are determined by the value of *K*; the third part corresponds to the three linear corner transistors (T3). There are only three T3, due to the presence of the polysilicon strip, which is necessary to integrate the gate contact outside the thin gate oxide region. Studies of the electric field under the gate of the device, supported by simulation and measurements, lead to the following formula [Gir00]:

$$\left(\frac{W}{L}\right)_{eff} = 4 \cdot \frac{2\alpha}{\ln\left(\dfrac{d'}{d'-2\alpha L_{eff}}\right)} + 2K \cdot \frac{1-\alpha}{\dfrac{1}{2}\sqrt{\alpha^2 + 2\alpha + 5} \cdot \ln\dfrac{1}{\alpha}} + 3 \cdot \frac{\dfrac{d-d'}{2}}{L_{eff}}, \tag{5.1}$$

where *c, d,* $d' = d - c\sqrt{2}$ and α are shown in Figure 5.1. L_{eff} is used in the equation to take into account the gate length shortening due to underdiffusion, photolithography and etching. *K* is a geometry-dependent parameter, used to take into account the number of T2's present in the ELT (Figure 5.1). The polysilicon strip has a constant width (A in Figure 5.1), which is independent of the transistor gate length, and is equal to the minimum gate length. The parameter *K* that multiplies the second term in (5.1) is geometry-dependent. For long channel devices (L greater than 0.5 μm) the *K* value is 4. When the channel width of transistors is shorter (L equal or less than 0.5 μm), the value of *K* is gradually changing from 4 to 3.5, since the polysilicon strip starts to "hide" one of the T2. α is a parameter that is needed to identify the borderline between transistors T1 and T2 in Figure 5.1. It is not possible to know a priori the value of α and its value is determined from a fit to the experimental data. After testing different CMOS technologies scaling from 2.5 μm to 0.25 μm, α has been found to be almost technology-independent, 0.05 being the best fit to the experimental data [Gir00]. The sum of the three addends gives the effective *W/L* of the ELT.

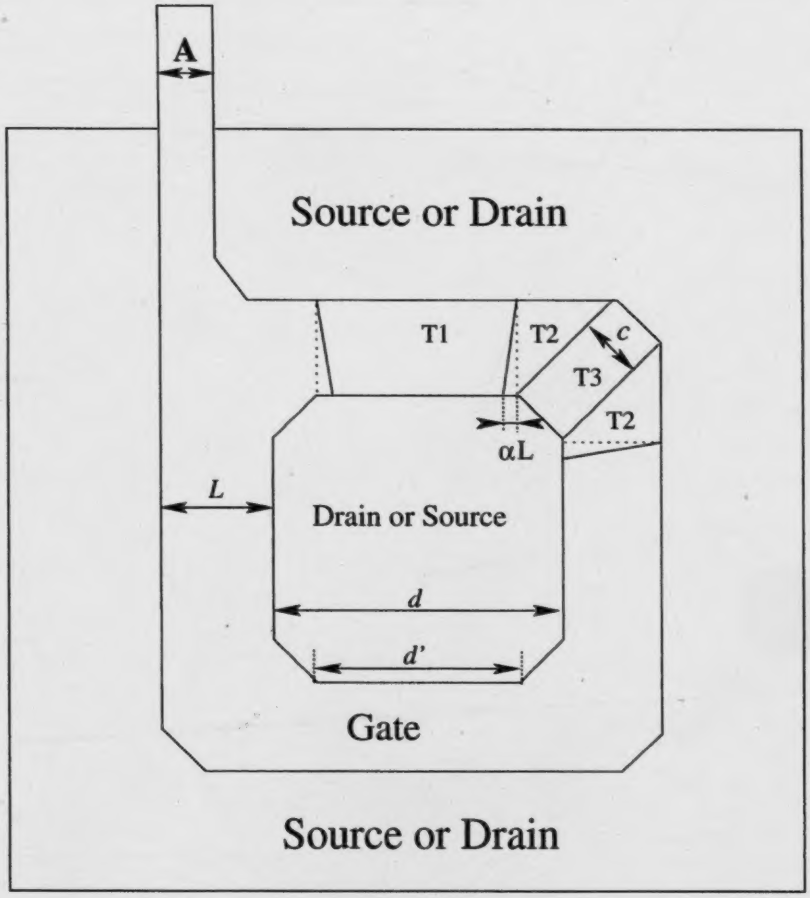


Figure 5.1: Diagram of an enclosed-gate transistor. The transistor can be thought of as being formed by transistors of three different kinds in parallel, labeled in the picture T1, T2 and T3. *L* remains the same for all sides.

The aspect ratio of *W/L* can be enlarged by stretching the layout in one (or the other) dimension. The shape is shown in Figure 5.2. In this case, one only needs to add the contribution of the linear regions generated by the stretching. The size of corners does not change when stretching. The formula used to calculate the *W/L* is the following:

$$\left(\frac{W}{L}\right)_{eff} = 2\cdot\frac{2\alpha}{\ln\left(\frac{d_l'}{d_l'-2\alpha L_{eff}}\right)} + 2\cdot\frac{2\alpha}{\ln\left(\frac{d'}{d'-2\alpha L_{eff}}\right)} + 2K\cdot\frac{1-\alpha}{\frac{1}{2}\sqrt{\alpha^2+2\alpha+5}\cdot\ln\frac{1}{\alpha}} + 3\cdot\frac{\frac{d-d'}{2}}{L_{eff}},\quad (5.2)$$

where the parameters, *d, d', d_l, d_l', L,* A are shown in the following diagram. The corner cut still remains 45°. The first two terms correspond to the two linear transistors in each direction.

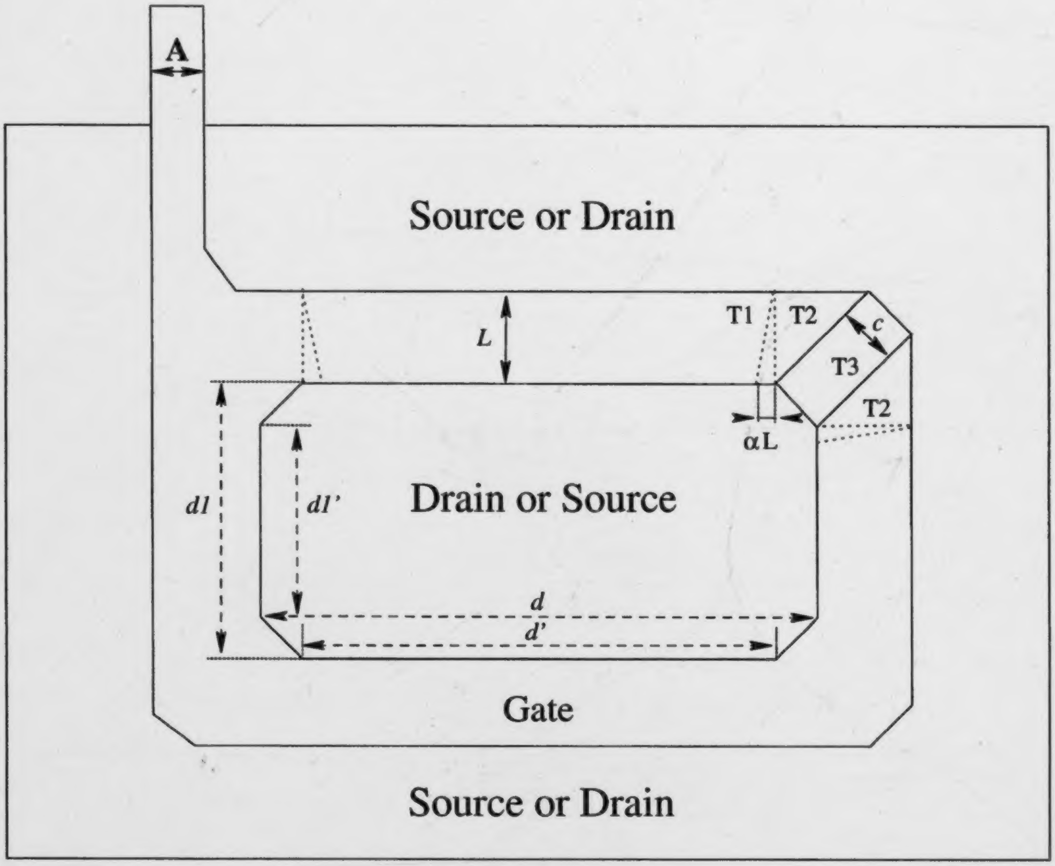


Figure 5.2: Shape of an enclosed-gated transistor stretched in one direction to achieve a higher aspect ratio.

5.2 *Verification*

The agreement between the formula and extracted aspect ratios was verified with a 0.18-μm technology, provided by Taiwan Semoconductor Manufacturing Company (TSMC). The 0.18-μm CMOS commercial process has the following features:

- Normal operation voltage: 1.8 V,
- Gate oxide thickness: 4.3 nm.

A design with enclosed-gate transistors and standard transistors was fabricated using this technology. During the investigation, two chips were tested.

5.2.1 Test chip development

First, the Diva Extraction Rules (DRC) written with the SKILL lanuage for standard transistors were modified so that the aspect ratio of an ELT could be extracted according to Equation 5.1.

Second, the layout of five different sizes of ELTs were laid out with Parameterized Cells using the SKILL lanuage in Cadence. The shape of the layout for ELTs is a square with the corners cut at 45°. The values of the parameters in Figure 5.1 are listed as follows:

- $d = 0.54$ μm,
- $c = 0.05$ μm,
- A = 0.18 μm.

The gate lengths of the five ELTs are 3 μm, 2 μm, 1 μm, 0.5 μm, and 0.21 μm respectively. Figure 5.3 shows three layout examples of the enclosed-gate transistors, whose gate lengths are 1 μm, 0.5 μm and 0.21μm respectively.

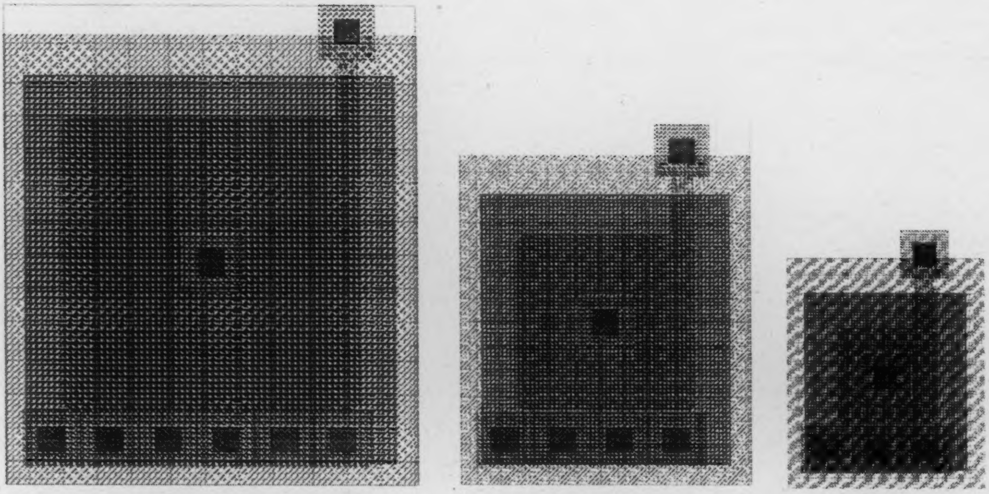

(A) (B) (C)

Figure 5.3: Layouts of three enclosed-gate transistors, whose gate lengths are 1 μm (A), 0.5 μm (B) and 0.21 μm (C), respectively. For each diagram, the blue square in the middle is the drain or source contact, surrounded with the gate (dark red). On the top of the layout, there is a gate contact and a squared-shaped piece of metal1. There are several contacts covered with metal1 for the source or drain at the bottom of the layouts.

The aspect ratios of ELTs were calculated and extracted according to Equation 5.1 with the parameters listed above using the modified extraction tool in Cadence, using the value of 0.05 for α. The drawn gate length was taked as L_{eff}. The calculated aspect ratios are listed in Table 5.1. From now on only the gate length of an ELT is indicated as each gate length corresponds to its own gate width. The behaviors of the transistors were simulated and their drain-source currents were measured using HSPICE simulations.

Standard transistors of the same size were also laid out with Parameterized Cells using the SKILL language. Finally all the developed devices were put into a design and fabricated.

Drawn Length (μm)	**Calculated Width (μm)**
3	7.9
2	5.9
1.0	3.9
0.5	2.9
0.21	2.3

Table 5.1: The drawn gate lengths and calculated widths for five sizes of enclosed-gate transistors.

5.2.2 Measurements and results

Enclosed-gate transistors and standard transistors were developed and fabricated into two set of chips named ELT# and STD#, where # indicates the number of the chips. The drain currents of all of enclosed-gate transistors and standard transistors in the corresponding chips (ELT0 and STD0) were measured. The effective aspect ratios of ELTs were extracted by comparing their drain current with the drain current of standard devices with the same L for the same gate bias of 0.8 V. The inner contact was used as the drain of ELTs. Since the effective aspect ratio for standard devices was known, the effective aspect ratios for the ELTs were extracted from the drain currents by comparing them to those of the standard ones. By operating the transistors at low drain voltage (0.05 V), the output conductance differences between standard layout transistor and ELT were minimized (more detailed information can be found in section 5.4). Table 5.2 shows that the differences between the calculated and measured aspect ratios are within 3 per cent. The results for one device show that the transistor model is still valid for the 0.18-μm CMOS technology without modifying the value of α (0.05). The test results for one device were based on two chips (one chip with standard transistors and one with ELT transistors) and therefore there could be some statistical variations.

Drawn Length (μm)	**Calculated Width (μm)**	**Extracted Width (μm)**	**Width Differences (per cent)**
0.21	2.34	2.32	-0.6
0.5	2.93	2.95	0.58
1	3.95	4.06	2.7
2	5.96	6.03	1.2
3	7.94	7.96	0.3

Table 5.2: Differences between the calculated and measured aspect ratios for five different sizes of enclosed-gate transistors, $V_{gs} = 0.8$ V, $V_{ds} = 0.05$ V. Extracted data are based on the measurement results from ELT0 and STD0.

A plot of the extracted enclose-gate transistor aspect ratio versus drawn channel length is show in Figure 5.4. Also shown in Figure 5.4 is a fit to the model of the aspect ratio in Equation 5.1. The results of the fit gave $\alpha = 0.053 \pm 0.001$.

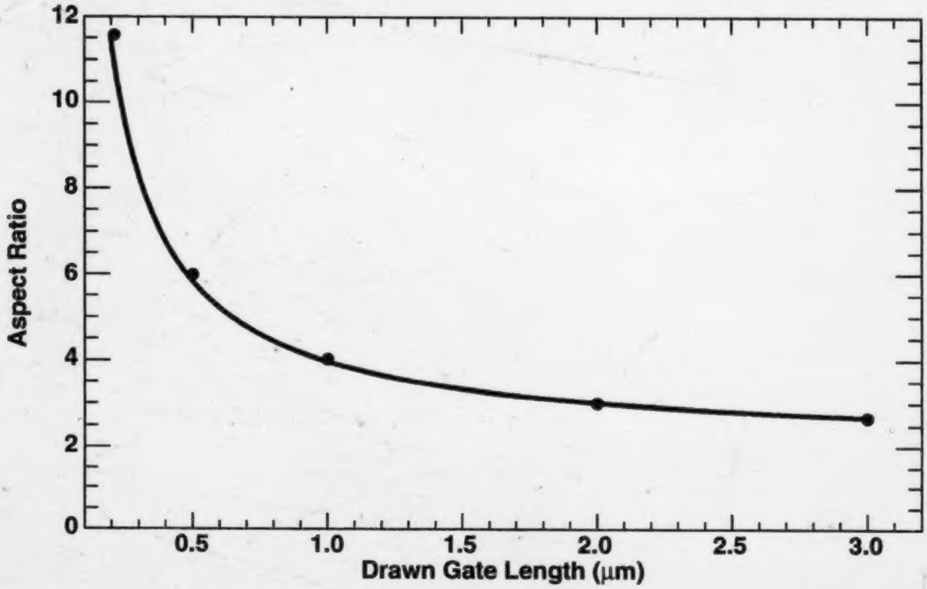


Figure 5.4: Extracted aspect ratio versus gate length. The curve is a fit to the data with α as a free parameter.

5.3 *Aspect ratio limitation*

From Equation 5.1 one can see that the aspect ratios cannot be lower than a certain value. To have lower aspect ratios the only way is to increase *L*, while keeping the minimum size for the distance *d*. However *W* is automatically increased when increasing *L*. Increasing *L* in Equation (5.1) causes the terms T1 and T3 to decrease, and after a certain value of *L* the term T2 will dominate. As it can be seen in Equation 5.1, the term T2 does not depend on *L* but only on α. Figure 5.5 shows the three addends of Equation 5.1 and the effective *W/L* as a function of the gate length. Each addend is equal to the product of each term indicated in Equation (5.1) and the number of times that the corresponding kind of transistor is present in the ELT (Figure 5.1). It can be seen that in the case of the geometry of Figure 5.1 the minimum *W/L* achievable is 2.26, and is reached with *L* larger than 4 µm. It should be pointed out that the gate area increases as the square of the gate length. Values close to the achievable minimum ratio also imply a considerable waste of area compared to the standard transistors and should be avoided by using different circuit topologies, i.e. using standard PMOS transistors.

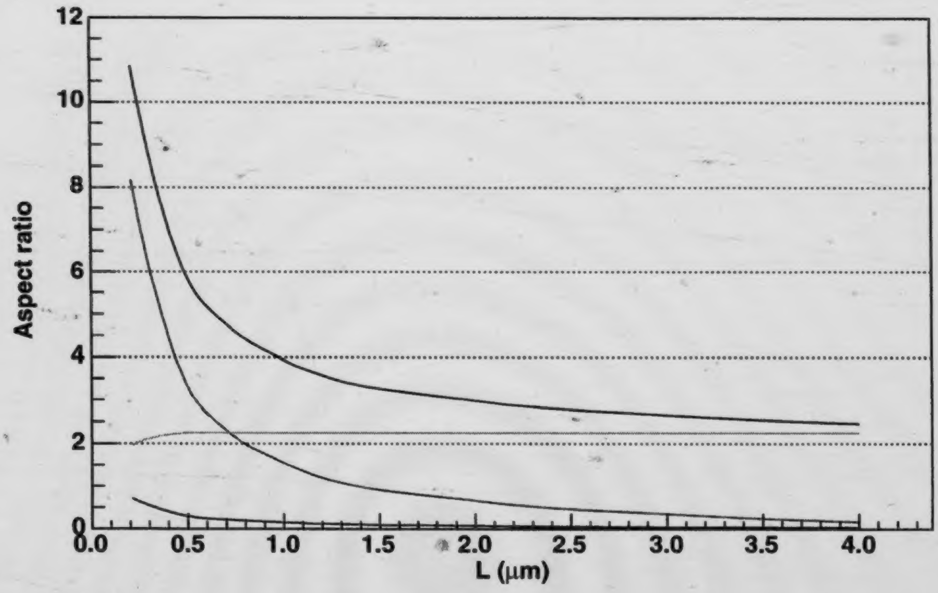


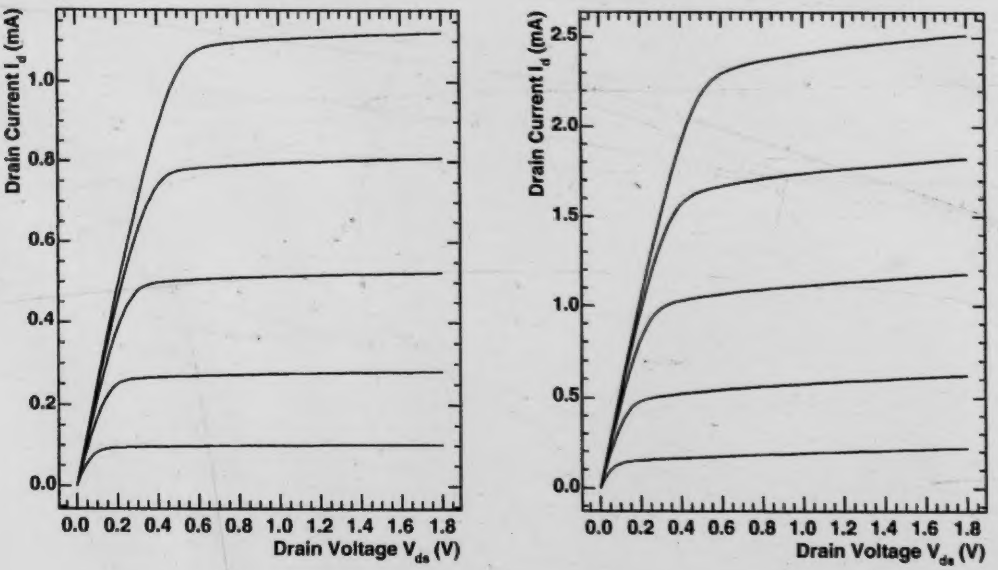
Figure 5.5: The first addend (red curve), the second addend (green curve), the third addend (blue curve) and the total (black curve) in Equation 5.1 as a function of the gate length.

It has been shown from the previous diagram that the minimum aspect ratio obtainable with the 0.18-μm CMOS technology is around 2.3, and this value is mainly determined by the second addend in Equation 5.1. This addend depends only on α, and K which is equal to 4 for long devices. One might wonder what will happen to the minimum aspect ratio achievable with the scaling of the technology. Assuming that the transistor shape of Figure 5.1 remains the same, Equation 5.1 still holds (i.e. there will not be new effects which will have to be taken into account). However, it is possible that the α parameter need to be adjusted in the new technology, and this will therefore change the minimum aspect ratio achievable. Increasing α will increase the minimum aspect ratio, whilst decreasing α, will decrease the minimum aspect ratio.

5.4 *Output characteristics*

The output characteristics have to be analyzed in order for ELT to be used in analog design. For a constant gate bias with V_{gs} greater than V_T, the drain current no longer increases with increasing drain voltage when the drain voltage reaches the pinch-off at the value of $V_{ds} = V_{gs} - V_T$, at which it is called the saturation drain voltage, V_{dsat}. However, the drain current still increases slowly after the pinch-off value, this is especially true for short channel transistors. The reason is that with the increased drain voltage the pinch-off point moves towards the source and reduces the effective channel length, which in turn increases the drain current. This phenomenon occurs in ordinary transistors and is called channel length modulation. It is also expect to be presented in ELT.

Figure 5.6 (A) and (B) shows two examples of drain current versus drain voltage characteristics for enclosed-gate transistors with two different gate lengths (L = 2 μm and 0.21 μm). Their gate widths can be found at Table 5.1. The gate voltages applied are 0.5 V, 0.6 V, 0.7 V, 0.8 V and 0.9 V, respectively. It is interesting to point out that the current slopes for short channel transistors (i.e. L = 0.21 μm) are larger than those of long channel transistors (i.e. L = 2 μm). This is because the distance ΔL between the pinch-off point and the drain diffusion is a smaller fraction of L for bigger devices, thus having less effect on the drain current.



(A) (B)

Figure 5.6: (A) $L = 2$ μm, $W = 5.96$ μm enclosed-gate transistor drain current versus drain voltage curves; (B) $L = 0.21$ μm, $W = 2.34$ μm enclosed-gate transistor drain current versus drain voltage curves. In every plot, the gate voltages of the five curves from bottom to top are 0.5 V, 0.6 V, 0.7 V, 0.8 V, and 0.9 V.

5.4.1 Output conductance asymmetry

The output conductance of the transistor, $g_d = \partial I_d / \partial V_{ds}$, is a very important parameter for analog designers. For example, the gain of a CMOS amplifier depends on this parameter. The lateral extension of the depletion layer around the drain diffusion into the channel region reduces the effective channel length. This depletion layer is bias-dependent and changes with the drain voltage modulating the effective channel length. Since the drain current depends on the channel length, its value depends not only on the gate voltage but also on the drain voltage through the effective channel length. For this reason the I_d versus V_{ds} characteristics of a MOS transistor in the saturation region are not level as they should ideally be, but show a slope.

Because of the non-symmetrical geometry of the ELT device, an asymmetry in the output conductance is observed. Since the gate is enclosed, the source and drain contacts can be chosen inside and outside the ring of the gate respectively, or vice versa. Table 5.3 shows the measured output conductance values for the drain inside (g_{di}) and outside (g_{do}). From the table, one can notice that g_{do} is lower than g_{di} and the differences increases with the gate length. The fact that g_{do} is lower can be explained to a first order as follows. The distance ΔL between the pinch-off point and the drain due to the conservation of the space charge region for the same bias potential is smaller when the drain is outside. Thus, an increase of V_{ds} will in this case increase less the drain current, resulting in a lower g_{do}. This fact can also be explained by comparing the equivalent width of the enclosed-gate transistors for the drain inside and outside the gate. The equivalent width is wider when the drain is inside. The asymmetry between g_{di} and g_{do} increases with L as the outer perimeter of the gate increases with L, which means that less ΔL will be introduced, while the inner one remains the same.

Width/Length (μm/μm)	g_{di} (μS)	g_{do} (μS)	Differences (per cent)
2.34/0.21	57.5	46.7	18.8
2.93/0.5	18.0	13.4	25.6
3.95/1.0	9.6	6.0	37.5
5.96/2.0	5.5	2.9	47.3
7.94/3.0	4.3	2.1	51.1

Table 5.3: The measured output conductance values for the drain inside (g_{di}) and outside (g_{do}) the gate with five different enclosed-gate transistor sizes. V_{gs} of the transistors is 0.5 V.

The charge region volumes of the two arrangements of the drain are the same, shown in Figure 5.7. This gives the following equation

$$W_{out} \cdot \Delta L_{do} - 4 \cdot \Delta L_{do}{}^2 = W_{in} \cdot \Delta L_{di} - 4 \cdot \Delta L_{di}{}^2, \tag{5.3}$$

where W_{out} is the outer gate perimeter (outside gate width times four) and W_{in} is the inner gate perimeter (inside gate width times four). Ignoring $\Delta L_{do}{}^2$ and $\Delta L_{di}{}^2$, one has

$$W_{out} \cdot \Delta L_{do} = W_{in} \cdot \Delta L_{di} . \tag{5.4}$$

Because W_{out} is greater than W_{in}, it is easy to conclude that $\Delta L_{do} < \Delta L_{di}$, which is demonstrated in table 5.3.

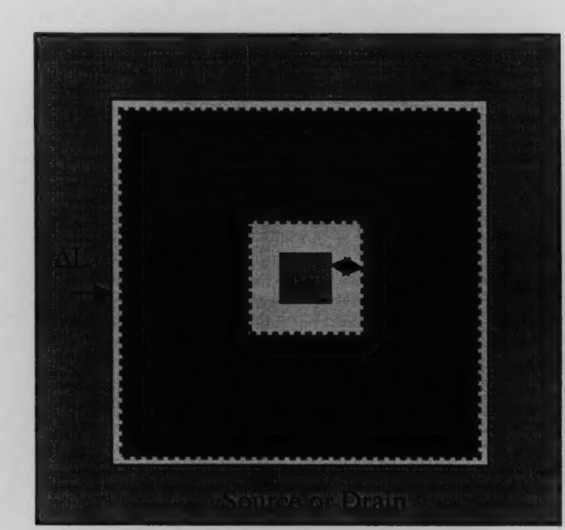


Figure 5.7: Illustration of the channel length modulation for an enclosed-gate transistor with the drain in or outside the gate. The dotted lines on the gate of the enclosed-gate transistor indicate the position of the pinch-off inside the channel for the two possible choices of the drain. A square gate was taken here to simplify the calculations.

5.4.2 Channel length modulation

In the SPICE Level 1 model, the channel length modulation is taken into account by the factor λ in such a way that:

$$I_d = I_d\big|_{Vdsat} \cdot (1 + \lambda \cdot V_{ds}). \qquad (5.5)$$

The level 1 λ extraction was made in the tested technology to evaluate the channel length modulation hypothesis. The extraction was made for each transistor, from the I_d versus V_{ds} curves with a given gate voltage, in the region with constant slope after the saturation voltage V_{dsat}. The extracted values of λ are different when the gate length is different. For shorter gate lengths λ is larger.

The data in Figure 5.8 confirms the hypothesis. It exhibits the extracted λ results from standard transistors (green curve), ELTs with the drain inside (black curve), ELTs with the drain outside (red curve). In this picture, it is clear that the symmetry is broken between the source and drain. λ is stronger when the drain is inside the gate than that of outside.

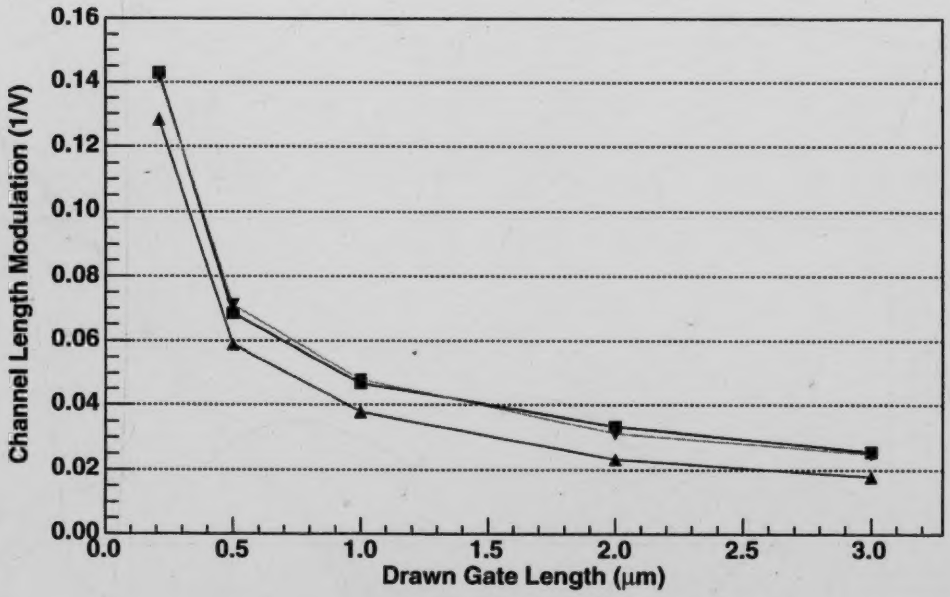


Figure 5.8: Channel length modulation data extracted from the standard transistors (green curve), enclosed-gate transistors with the drain inside (black curve) and source inside (red curve) configurations, V_{gs} = 0.9 V. For each type of transistors, there are five different gate lengths, 3.0 μm, 2.0 μm, 1.0 μm, 0.5 μm and 0.21 μm.

Chapter 6 Total Dose Effects on Enclosed-GateTransistors

In this chapter, total dose effects on enclosed-gate transistors are studied. Radiation test procedures are described in section 6.1. The pre-irradiation parameters, threshold voltage, subthreshold slope and leakage current for each transistor, are listed in section 6.2. The radiation-induced threshold voltage shift of different length transistors is presented in section 6.3. The subthreshold slope is important in the analysis of the threshold voltage shift introduced by SiO_2-Si interface. This is discussed in section 6.4. The radiation-induced leakage current of enclosed-gate transistors with guard rings is measured and presented in section 6.5. In section 6.6, the transconductance, g_m, before and after irradiation is extracted and reported.

6.1 Radiation test procedures

Five chips were tested before and after irradiation. Every chip had six types of enclosed-gate transistors with different aspect ratios. Fifty transistors were connected in parallel for each type of transistors. All of the measured results are divided 50 before analyzing the data. Their width and length are listed in Table 6.1. The detailed information of the enclosed-gate transistors was described in the previous chapter.

Length (μm)	Width (μm)
3	7.94
2	5.96
1.5	4.96
1.0	3.95
0.5	2.93
0.21	2.34

Table 6.1: The width and length of enclosed-gate transistors in each chip under test.

The irradiations were performed using an X-ray facility located in the Centre of

Subatomic Research at the University of Alberta [Gin], using dose rates of 0.48 +/- 0.03 Gy(SiO_2)/s. Devices were kept at room temperature under the worst-case bias during irradiation ($V_{gs} = 1.8$ V for NMOS transistors and $V_{gs} = 0$ V for PMOS transistors; $V_{ds} = V_{bs} = 0$ V in both cases). The worst-case means that the positive electric field is the maximum across the gate.

DUTs were irradiated for different time periods. Between every period, measurements were made within an hour. The I_d - V_{ds} and I_d - V_{gs} curves were obtained using an Agilent Parameter Analyzer 4155. Table 6.2 shows the radiation periods and radiation doses received by each DUT.

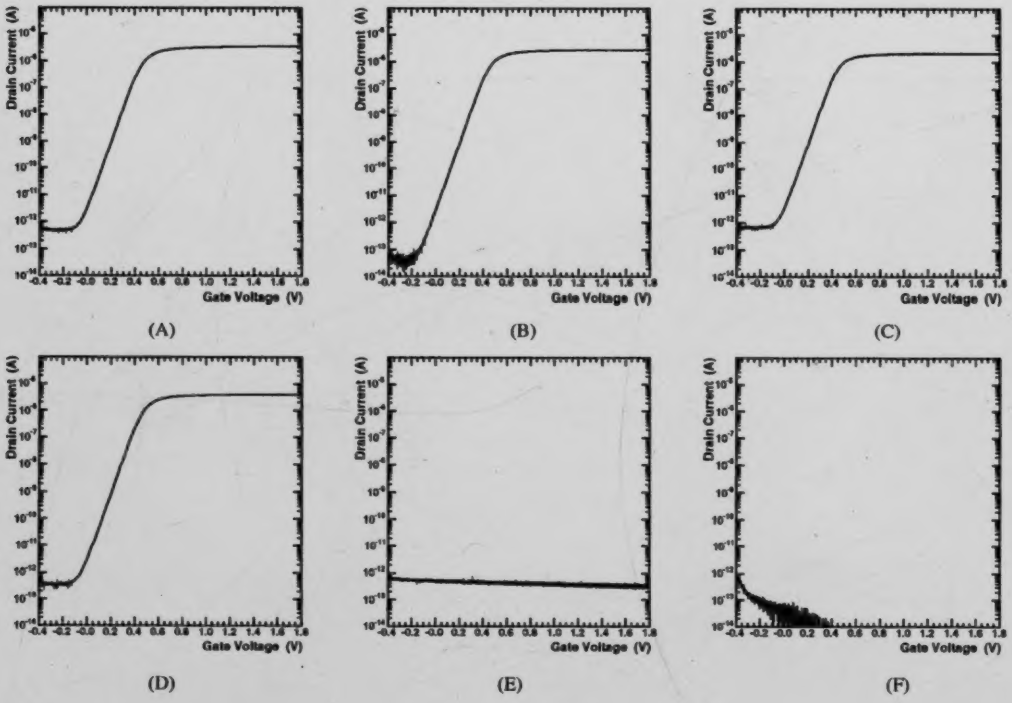
Annealing was performed after the irradiation for one chip, one day at room temperature and one week at 100° C.

DUT number	**Radiation time and absorbed dose**	**1st period**	**2nd period**	**3rd period**	**4th period**	**5th period**
0	Irradiation time (hour)	1	2.5	5	9.5	16.5
	Total Dose (kGy)	1.8±0.1	4.6±0.3	9.0±0.6	16.9±1.0	29.0±1.8
1	Irradiation time (hour)	1	3	7	16	35
	Total Dose (kGy)	1.6±0.1	5.1±0.3	12.8±0.8	28.3±1.8	60.7±3.8
2	Irradiation time (hour)	1	2.5	5	8.5	
	Total Dose (kGy)	1.7±0.1	4.7±0.3	9.5±0.5	14.9±0.9	
3	Irradiation time (hour)	1	3	8	18	41
	Total Dose (kGy)	1.7±0.1	5.0±0.3	13.9±0.9	31.4±2.0	71.1±4.5
4	Irradiation time (hour)	1	3	7	15	29
	Total Dose (kGy)	1.7±0.1	5.2±0.3	12.1±0.8	26.0±1.7	50.3±3.2

Table 6.2: The radiation time periods and radiation doses absorbed by each chip under test.

6.2 Devices before irradiation

The drain current versus gate voltage data for each transistor in the circuit was measured before and after every irradiation period. An example of six I_d - V_{gs} curves measured from DUT3 (received the highest total ionizing dose) before irradiation is shown in Figure 6.1. The drain to source voltage is 0.05 V. The I_d is plotted on a log scale to show the exponential increase of subthreshold current with gate voltages less than V_T (about 0.4 V).



(A) (B) (C)

(D) (E) (F)

Figure 6.1: Drain current versus gate voltage data for six transistors whose gate lengths are (A) 3 μm, (B) 2 μm, (C) 1.5 μm, (D) 1 μm, (E) 0.5 μm, (F) 0.21 μm in DUT3. The drain to source voltage is 0.05 V.

Results from some transistors show a strange trend, for example, the $L = 0.21$ μm and $L = 0.5$ μm transistors in DUT3. The curves of these transistors showed that they were damaged before irradiation. The results of these transistors were not analyzed. Transistor damage has been regarded as the static electricity during testing. The ESD protection circuits were deliberately not connected to the transistors when laying the transistors to avoid the unwanted leakage currents caused by protection circuits. The bad transistors are listed in Table 6.3.

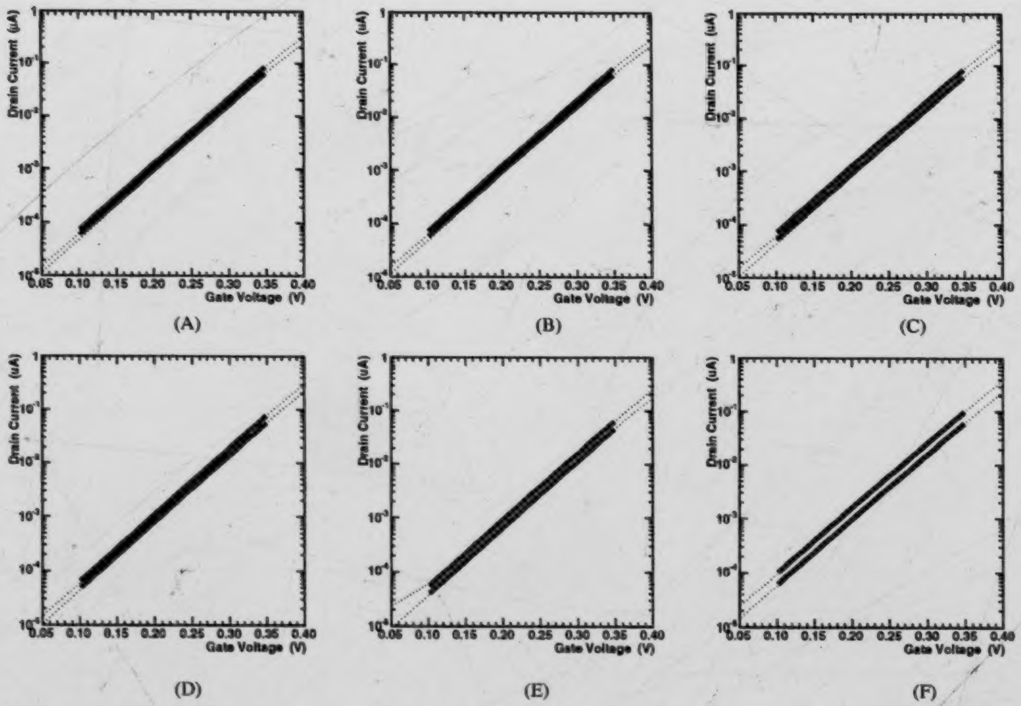
DUT Number	Damaged Transistors
0	L = 0.21μm, L = 0.5 μm
1	L = 0.21μm, L = 0.5 μm, L = 1.5 μm
2	L = 0.21μm
3	L = 0.21μm, L = 0.5 μm
4	None

Table 6.3: List of damaged enclosed-gate transistors not caused by irradiation.

The threshold voltage was extracted from the I_d - V_{gs} curves, by finding the maximum slope from the curves. This method is a common method to extract V_T [Sch90]. The pre-irradiation threshold voltage was extracted from the I_d - V_{gs} curve for each enclosed-gate transistor. The mean and rms deviation for each threshold voltage is shown in Table 6.4. The average threshold voltage was (399±4) mV.

The subthreshold slope shift was extracted from the log scale I_d versus V_{gs} curves, in which the subthreshold current can be fit to a straight line to find the slope in the range of 0.10 V to 0.35 V for V_{gs}. An example of fitting diagrams of DUT4 is shown in Figure 6.2. The two dotted lines in each diagram are the current data when V_{ds} are 0.05 V and 1.0 V respectively. The solid thick lines are the fit results.

The pre-irradiation mean and rms deviation of the subthreshold swing (inverse of the subthreshold slope) for each enclosed-gate transistor is shown in Table 6.4. The average subthreshold swing was (81.8 ± 0.4) mV/decade.



(A) (B) (C)

(D) (E) (F)

Figure 6.2: In the subthreshold region, drain current (on log scale) versus gate voltage, fitted to a straight line for six types of transistors in DUT4. The gate lengths of the transistors are (A) 3 μm, (B) 2 μm, (C) 1.5 μm, (D) 1 μm, (E) 0.5 μm and (F) 0.21 μm. The two lines represent data of drain current when the drain voltages are 0.05 V and 1 V, respectively. The line on the top is for V_{gs} = 1 V in each diagram.

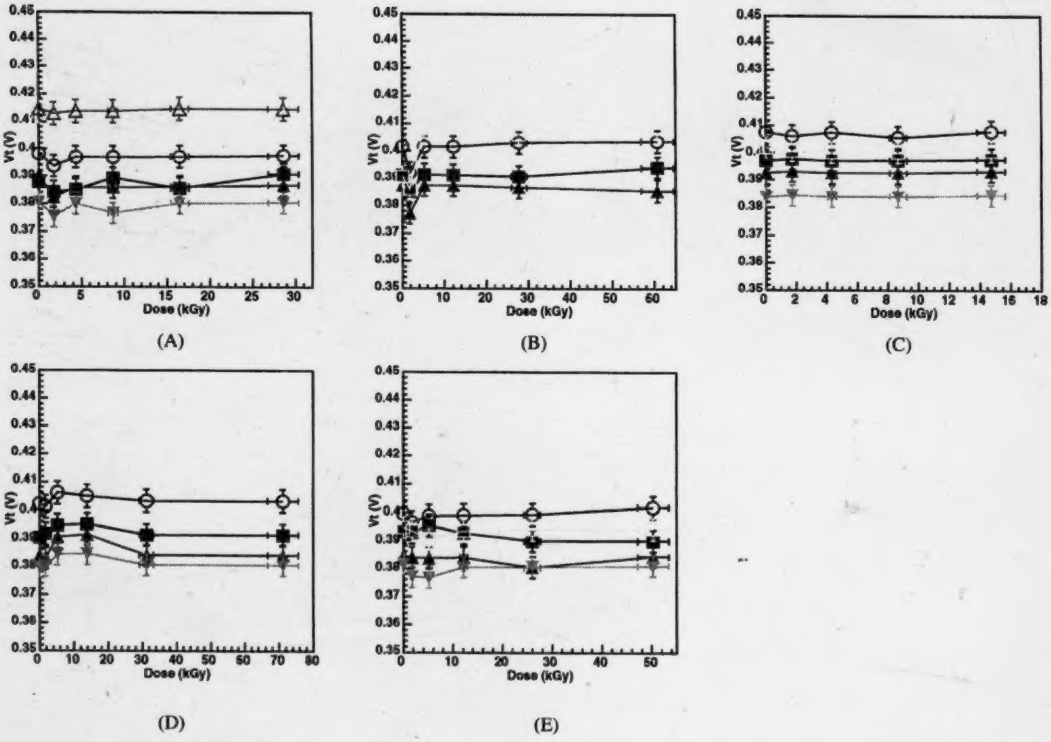
The leakage current is extracted when V_{gs} = 0 V and V_{ds} = 1 V. The mean and rms deviation of the leakage current before irradiation for each enclosed-gate transistor size are shown in Table 6.4. The average leakage current was 9 pA.

L (mm)	V_T (mV)	Subthreshold Swing (mV/decade)	Leakage Current (nA)
3.00	393±3	81.9 ±0.2	0.014 ±0.020
2.00	388 ±4	82.0 ±0.2	0.008 ±0.010
1.5	381 ±1	82.0 ±0.5	0.004 ±0.001
1.00	402 ±4	81.0 ±0.2	0.011 ±0.015
0.50	398 ±5	81.2 ±0.5	0.010 ±0.006
0.21	430	83.0	0.006

Table 6.4: The pre-irradiation mean and RMS of the threshold voltage, V_T, subthreshold swing, and leakage current for each enclosed-gate transistor.

6.3 Radiation-induced threshold voltage shift

The threshold voltage shift as a function of the total dose for each DUT is shown in Figure 6.3, in which each color line indicates the data of one type of transistor. The black, red, green, blue, yellow and pink curves represent the data of $L = 3.0$ μm, $L = 2.0$ μm, $L = 1.5$ μm, $L = 1.0$ μm, $L = 0.5$ μm, $L = 0.21$ μm transistors, respectively. One can conclude that the shift of threshold voltage for these ELT transistors is less than 2% up to 70 kGy(SiO_2) total dose. This is a very promising result for radiation applications.



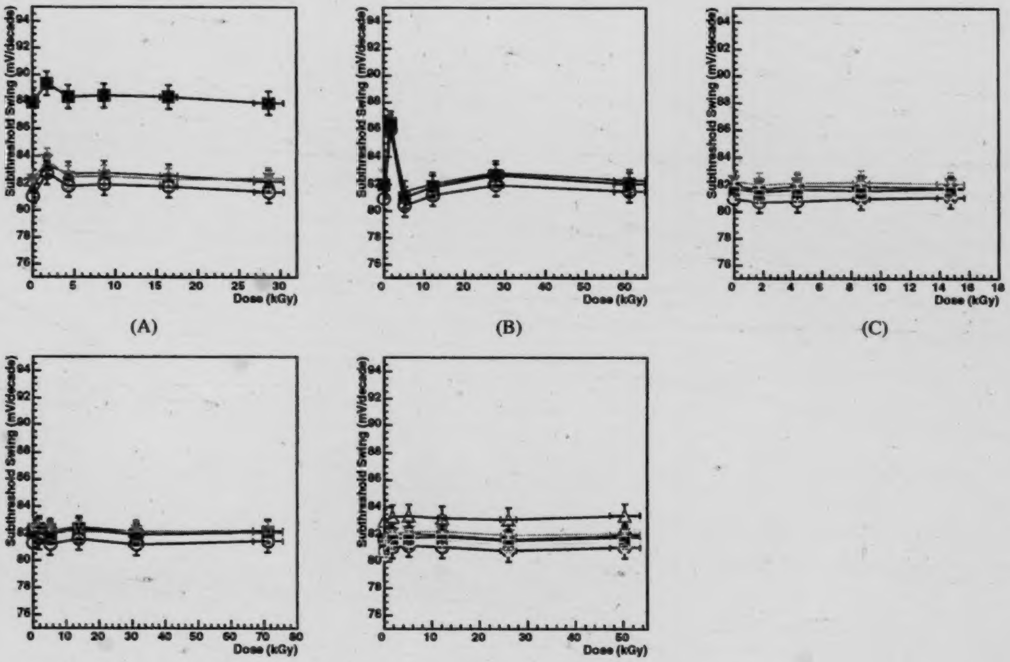
(A) (B) (C)

(D) (E)

Figure 6.3: The threshold voltage shift as a function of the total dose for the transistors in DUT0 (A), DUT1 (B), DUT2 (C), DUT3 (D) and DUT4 (F). In each diagram, the black, red, green, blue, yellow and pink curves represent the data of $L = 3.0$ μm, $L = 2.0$ μm, $L = 1.5$ μm, $L = 1.0$ μm, $L = 0.5$ μm, $L = 0.21$ μm enclosed-gate transistors, respectively. Some curves of the damaged transistors are not present.

6.4 Radiation-induced subthreshold swing shift

The extracted subthreshold swings as a function of dose for each DUT are shown in Figure 6.4.



(A)

(B)

(C)

(D)

(E)

Figure 6.4: The extracted subthreshold swing as a function of the total dose for the transistors in DUT0 (A), DUT1 (B), DUT2 (C), DUT3 (D) and DUT4 (E), $V_{gs} = 0.05$ V. In each diagram, the black, red, green, blue, yellow and pink curves represent the data of $L = 3.0$ μm, $L = 2.0$ μm, $L = 1.5$ μm, $L = 1.0$ μm, $L = 0.5$ μm, $L = 0.21$ μm enclosed-gate transistors, respectively.

From Equation 2.2, ΔV_{it} can be calculated and the results are listed in Table 6.5. As ΔV_T is known from previous section 6.2, ΔV_{ox} can be calculated by subtracting ΔV_{it} from ΔV_T. From the table, it shows generally that ΔV_{ox} contributes a negative shift to the ΔV_T and that of ΔV_{it} is opposite, although the shift is insignificant.

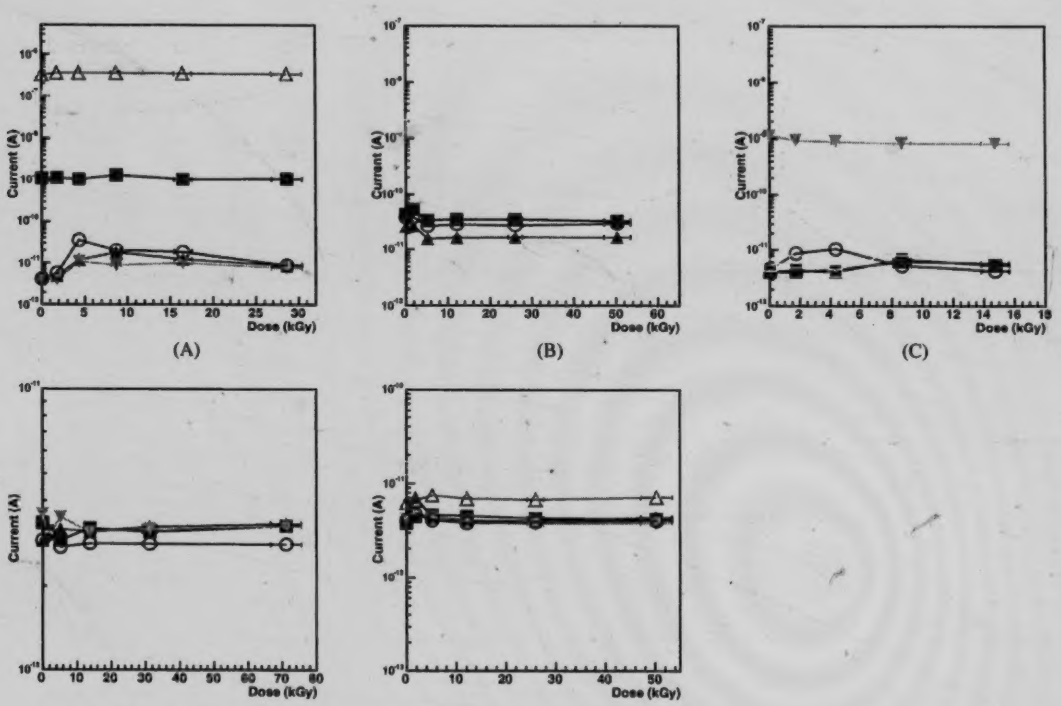
DUT#	Shift of Parameters	L=3 µm	L=2 µm	L=1.5 µm	L=1 µm	L=0.5 µm	L=0.21 µm	Mean and RMS
DUT0	**ΔV_T (mV)**	3.0	-3.41	0	-0.50	-	-	-0.23±2.62
	ΔS (mV/decade)	-0.02	0.47	0.14	0.34	-	-	0.23±0.21
	ΔV_{it} (mV)	-0.17	3.49	1.06	2.52	-	-	1.73±1.54
	ΔV_{ox} (mV)	3.17	-6.90	-1.06	2.02	-	-	-0.69±4.23
DUT1	**ΔV_T (mV)**	2.83	-1.82	-	2.01	-	-	1.01±2.38
	ΔS (mV/decade)	0.087	0.21	-	0.58	-	-	0.29±0.16
	ΔV_{it} (mV)	0.64	1.54	-	4.25	-	-	2.14±1.15
	ΔV_{ox} (mV)	2.19	-3.36	-	-2.24	-	-	-1.14±2.83
DUT2	**ΔV_T (mV)**	0.51	0.63	0.62	0.41	-1.31	-	0.17±0.38
	ΔS (mV/decade)	0.02	-0.15	-0.17	0.12	0.06	-	-0.02±0.12
	ΔV_{it} (mV)	0.16	-1.15	-1.24	0.89	0.45	-	0.78±0.43
	ΔV_{ox} (mV)	0.35	1.78	1.86	-0.45	-1.76	-	0.36±1.11
DUT3	**ΔV_T (mV)**	4.62	6.91	4.92	3.34	-	-	4.95±1.15
	ΔS (mV/decade)	0.02	-1.3	-0.24	0.15	-	-	-0.34±0.59
	ΔV_{it} (mV)	0.17	-0.96	-1.76	1.11	-	-	-0.36±0.93
	ΔV_{ox} (mV)	-0.15	7.87	6.68	4.45			4.69±3.35
DUT4	**ΔV_T (mV)**	-2.83	0	-0.55	1.42	-0.41	0	-0.40±1.37
	ΔS (mV/decade)	0.18	0.14	0.78	0.31	0.59	0.41	0.42±0.25
	ΔV_{it} (mV)	1.34	1.05	5.71	2.30	4.38	2.98	2.96±1.8
	ΔV_{ox} (mV)	-4.17	-1.05	-6.27	-0.88	-4.79	-2.98	-3.36±2.13

Table 6.5: List of ΔV_T, subthreshold swing shift, ΔV_{it}, and ΔV_{ox} for each transistor after irradiation.

6.5 Radiation-induced leakage current

The radiation-induced turn on of parasitic MOS devices can occur in the circuit because the field oxide is more sensitive to oxide charge trapping than thinner gate oxide. The V_T shift of these parasitic transistors can be very large. Their turn on gives leakage paths that can compromise the isolation of the devices or parts of a single device. This could cause the failure of the devices. This phenomenon depends on the device's geometry because it occurs when the field oxide is placed near the channel and underneath the polysilicon gate or metal lines, and it can be suppressed with layout modification. The enclosed-gate NMOS transistors can effectively eliminate any source-drain leakage path.

The extracted leakage currents as a function of dose for each DUT are shown in Figure 6.5. The black, red, green, blue, yellow and pink curves represent the data of $L = 3.0$ µm, L= 2.0 µm, $L = 1.5$ µm, $L = 1.0$ µm, $L = 0.5$ µm, $L = 0.21$ µm enclosed-gate transistors, respectively.



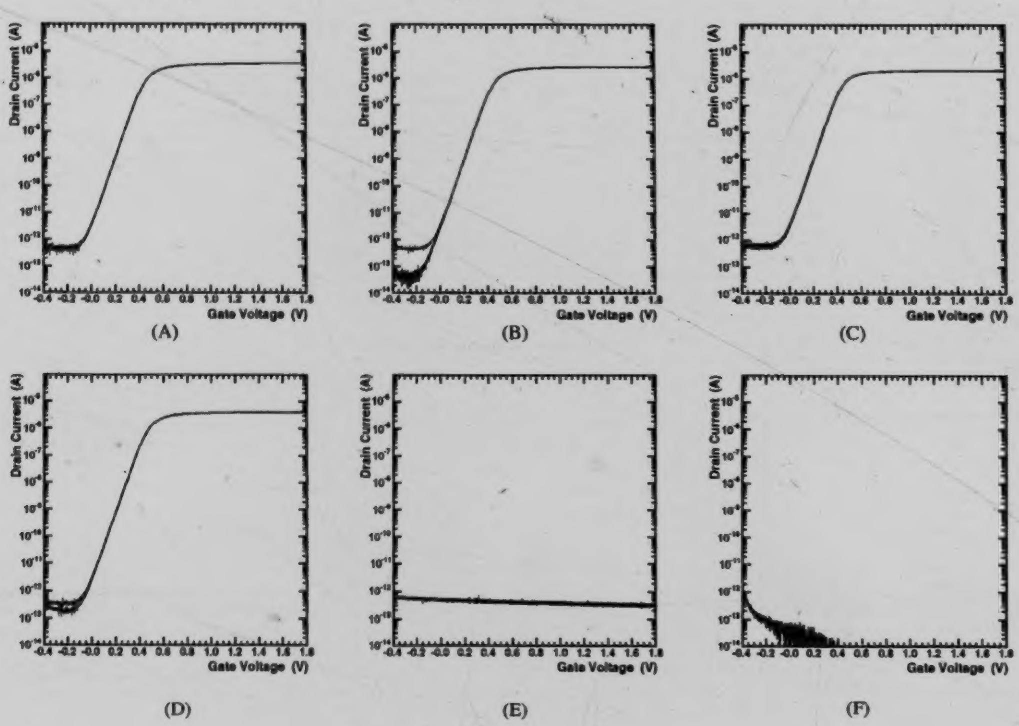
(A) (B) (C)

(D) (E)

Figure 6.5: The leakage current as a function of the total dose for the transistors in DUT0 (A), DUT1 (B), DUT2 (C), DUT3 (D) and DUT4 (E). In each diagram, the black, red, green, blue, yellow and pink curves represent the data of enclosed-gated transistors whose gate lengths equal 3.0 µm, 2.0 µm, 1.5 µm, 1.0 µm, 0.5 µm and 0.21µm, respectively. The drain voltage is 1.0 V, and the gate voltage is 0 V for each transistor.

6.6 Radiation-induced transconductance shift

Transconductance is an important parameter in analog circuit design. It is necessary to observe the changes induced by radiation. An example of I_d-V_{gs} curves before and after irradiation for the enclosed-gate transistors in DUT3 is presented in Figure 6.6. One can observe that the differences due to radiation are too small to be observed except for V_{gs} less than zero.



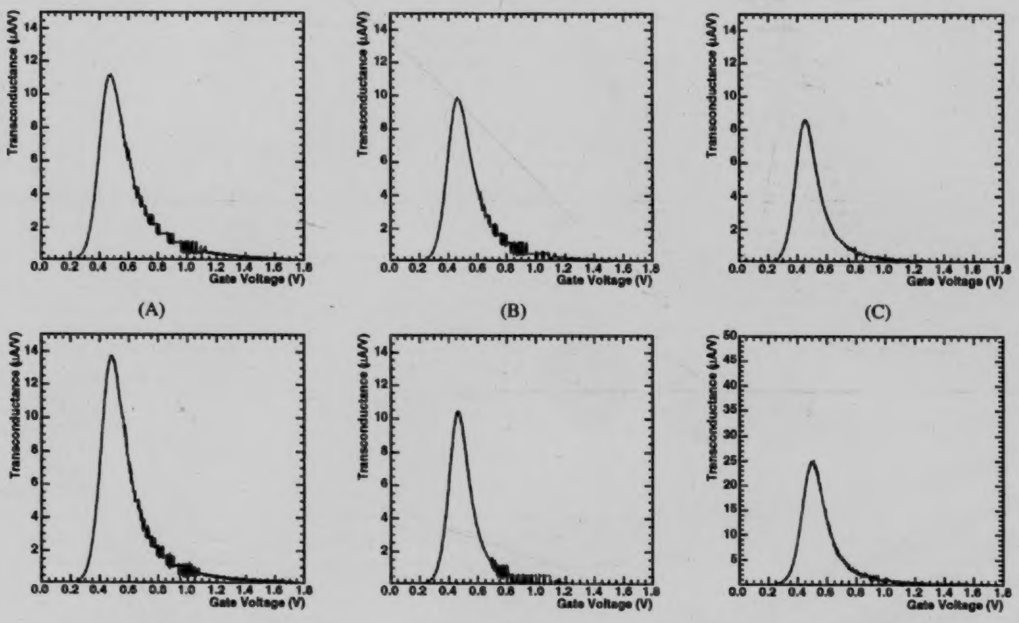
(A) (B) (C)

(D) (E) (F)

Figure 6.6: An example the of drain current versus gate voltage curves before (black curve) and after 70 kGy(SiO_2) irradiation (red curve) for six different sizes of transistors in DUT3. The gate lengths for the tested transistors are (A) 3 μm, (B) 2 μm, (C) 1.5 μm, (D) 1 μm, (E) 0.5 μm, (F) 0.21 μm. The drain voltage is 0.05 V.

The transconductance was extracted from the I_d - V_{gs} data. To be specific, ΔI_d is divided by ΔV_{gs} for every small step of V_{gs} (0.002 V) to obtain the corresponding transconductance.

Figure 6.7 shows that the extracted g_m curves from six different size enclosed-gate transistors before and after 50 kGy(SiO_2) irradiation. A specific example is shown in Figure 6.8, which displays the extracted g_m curves from an enclosed-gate transistor whose gate length is 0.21 μm. As expected from I_d -V_{gs} curves, the transconductance of NMOS ELT transistors is affected by irradiation to a very limited extent which almost cannot be observed. It shows a very promising prospect for analog designers.



(A)

(B)

(C)

(D)

(E)

(F)

Figure 6.7: Extracted transconductance curves before (black) and after (green) 50 kGy(SiO_2) irradiation for different size enclosed-gate transistors in DUT4. The gate lengths for the tested transistors are (A) 3 μm, (B) 2 μm, (C) 1.5 μm, (D) 1 μm, (E) 0.5 μm, (F) 0.21 μm. The drain voltage is 0.05 V.

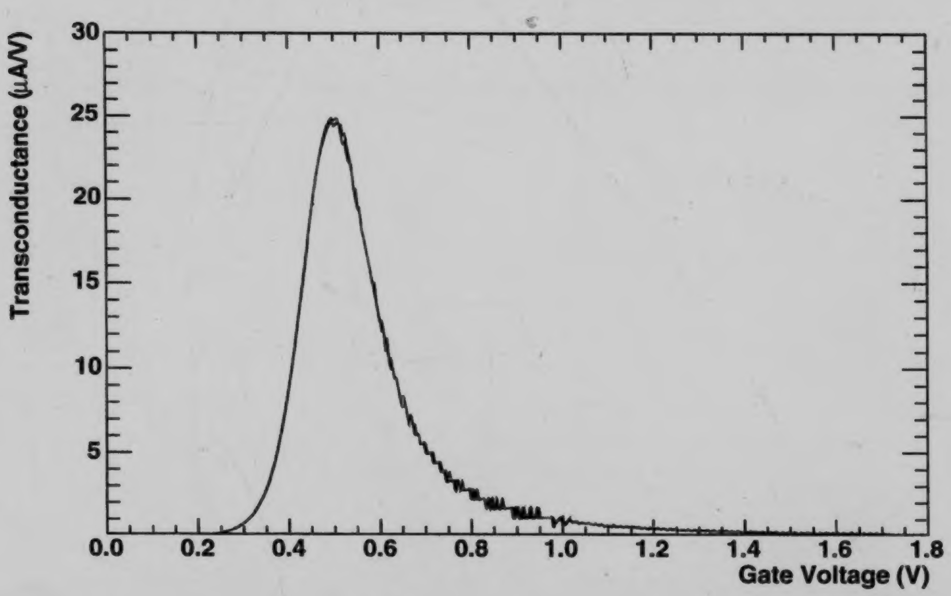


Figure 6.8: Extracted transconductance curves before (black) and after (green) 50 kGy(SiO_2) irradiation for an enclosed-gate transistor in DUT4. The gate length for the tested transistor is 0.21 µm. The drain voltage is 0.05 V.

Chapter 7 Noise Performance of Enclosed-Gate Transistors

Deep submicron CMOS technologies are receiving more interest in the design of ASICs to be used in many harsh radiation environments. The aspects relevant to the use of these advanced technologies for analog applications have to be investigated. In this chapter the studies are focused on the noise performance of enclosed-gate transistors that is of paramount importance for the design of low-noise analog amplifiers. The noise performance of deep submicron processes is highly technology-dependent and therefore it is extremely important to perform noise characterization before using a given technology for the design of low-noise ICs. The noise spectra was measured for ELT transistors using a 0.18-μm CMOS technology in the bandwidth 10 kHz to 10 MHz, before and after irradiation. The aim of this study is to verify whether the noise performance of this type of transistor is suitable for low-noise front-end circuits used in particle physics experiments and how the noise is affected by irradiation.

The main noise sources in an MOS transistor are reviewed in section 7.1, and the test structures and the measurement systems are explained in section 7.2. In section 7.3, the noise performance results of the chosen transistors are presented. The $1/f$ and white noise are measured for NMOS enclosed-gate transistors. The noise degradation is measured after different levels of ionizing radiation.

7.1 MOSFET noise

The noise theory of MOSFETs is briefly reviewed in this section [Vit96, Tsi99, Cha91, Jin84, Mcw56]. The noise sources that are considered are the channel thermal noise and the $1/f$ noise. In the following subsections, these components will briefly be discussed and the formulae used during the analysis will also be introduced.

7.1.1 Channel thermal noise

The channel thermal noise is generated by the random thermal motion of the carriers in the channel. For a ideal long device in strong inversion and in saturation, the drain current power spectral density[2] can be expressed with the following formula [Vit96]:

$$\frac{\overline{I_{dsi}^{2}}}{\Delta f} = 4KT\frac{2}{3}(g_m + g_{mb}), \tag{7.1}$$

where K is Boltzmann's constant, T is the absolute temperature, g_m is the gate small-signal transconductance and g_{mb} the bulk small-signal transconductance. Dividing Equation 7.1 by $g_m^{\ 2}$ (assuming a zero source impedance), one obtains the input noise power spectral density generated by the resistive MOS channel:

$$\frac{\overline{V_{in}^{2}}}{\Delta f} = 4KT\frac{2}{3}\frac{1}{g_m}\frac{g_m + g_{mb}}{g_m} \approx 4KTn\frac{2}{3}\left(\frac{1}{g_m}\right), \tag{7.2}$$

where n is proportional to the inverse of the subthreshold slope and is larger than unity. Typically n is between 1 and 1.5, and is generally valid in weak, moderate and strong inversion. More details about the definition of n for various inversion conditions and on the relationships between n, g_m and g_{mb} can be found in [Tsi99 (pp. 75, 86, 101, 111-112, 369, 379, 382)].

For a device in weak inversion, the drain current power spectral density of the channel thermal noise can be given as [Rei82, Tsi99 (pp. 421, 426-427)]:

$$\frac{\overline{I_{dwi}^{2}}}{\Delta f} = 2qI_d\ , \tag{7.3}$$

where q is the electronic charge and I_d is the drain current. In weak inversion, g_m can be expressed as

$$g_m = \frac{I_d}{n\phi_t} , \tag{7.4}$$

where $\phi_t = kT/q$, is the thermal voltage. After manipulation, one has:

$$\frac{\overline{V_{in}^{\,2}}}{\Delta f} = \frac{2qI_d}{g_m^{\,2}} = 4KTn\frac{1}{2}\left(\frac{1}{g_m}\right) . \tag{7.5}$$

From (7.2) and (7.5), the input referred channel thermal noise in saturation and in any inversion region can thus be expressed in one expression as:

$$\frac{\overline{V_{in}^{\,2}}}{\Delta f} = 4KTn\gamma\left(\frac{1}{g_m}\right) , \tag{7.6}$$

where γ varies from 1/2 to 2/3 from weak to strong inversion. From Equation 7.6, one can observe that the thermal noise of a transistor depends on its transconductance. Equation 7.6 is valid for long-channel devices. For channel lengths less than 1 μm [Abi86], thermal noise is several times larger than the value given by Equation 7.6.

7.1.2 1/*f* noise

According to the McWorther model [Mcw56], the 1/*f* (or flicker) noise, is due to random trapping and de-trapping of mobile carriers in the traps located at the SiO_2-Si interface and within the gate oxide. It is the dominating source of noise of an MOS device at low frequencies and its input power spectral density is given by [Cha91 (p. 20)]:

$$\frac{\overline{V_{1/f}^{\,2}}}{\Delta f} = \frac{K_a}{C_{ox}\,WL}\cdot\frac{1}{f^{\alpha}} , \tag{7.7}$$

where α is a parameter close to 1 and K_a is a technology-dependent parameter which expresses the noise characteristic of the process. K_a should be constant for devices from a given process. Its value may be different for NMOS and PMOS transistors.

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[2] The characteristic which is independent of the measurement device bandwidth is called power spectral density [Fil]. It is measured in V^2/Hz or I^2/Hz.

7.1.3 Total noise power spectral density

Adding together the two noise contributions described above, the input referred noise power spectral density can finally be expressed as:

$$\frac{\overline{V_{in}^{2}}}{\Delta f} = 4KTn\gamma\left(\frac{1}{g_m}\right) + \frac{K_a}{C_{ox}WL}\cdot\frac{1}{f^{\alpha}}. \tag{7.8}$$

From the above analysis, one concludes that the overall noise consists of two terms[3]. The first term is the channel thermal noise, which does not change with the frequency. The second term is 1/*f* noise, which varies with the frequency. One can extract parameters K_a and α by fitting the noise data to a function which has a constant term and a term varying with frequency.

7.2 Experiment

The devices under test are described in section 7.2.1. The test setup for noise measurement is described in section 7.2.2 and the results are presented in section 7.2.3.

7.2.1 Devices under test

Wide devices are often needed in front-end circuits for high-energy physics experiments since signal over noise optimization requires matching of the detector capacitance and of the preamplifier input transistor capacitance [Sel87]. Wide transistors were used to achieve a sufficiently high white noise density in current at the drain (which allows one to perform more precise noise measurements). Large area devices also have a lower input referred 1/*f* noise (for a fixed g_m), allowing better measurement in the white noise region. There were three types of wide transistors, NMOS enclosed-gate transistors, NMOS standard transistors, and PMOS standard transistors in each test chip. Each type has three different gate lengths (0.21 μm, 0.5 μm and 1 μm). All of the wide transistors have the same equivalent width (200 μm). The noises of some small aspect ratio NMOS ELTs were also tested.

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[3] There are some other noise sources in a transistor, such as gate resistance and bulk resistance. However the contribution of these noises is much less significant than thermal noise and is thus safely ignored [Man02a].

7.2.2 Measurement setup

The schematic of the noise measurement setup is shown in Figure 7.1. The noise current at the drain of the transistor is measured with a transimpedance amplifying stage, which uses a low-noise wide-band operational amplifier. The resistor in Figure 7.1 is used to adjust the gain of the transimpedance stage. After a second gain stage, the output of the circuit is read with a Spectrum Analyzer (HP8590). Each noise measurement is done in three different steps. During the first step, the gain of the connection that consists of the DUT and the two amplifying stages is measured. To do that, the spectrum analyzer injects at the input of the circuit a signal whose amplitude is known and measures the output V_{out} of the chain. Repeating this procedure for different frequencies f and calculating the ratio between the output and the input signals gives the gain $G(f)$ as a function of the frequency. During the second step, the noise of the transistor amplified through the two gain stages (V_{TOT}) is measured. For the third step, the DUT bias circuitry is switched off, keeping on the power supplies of the two amplifying stages. The background noise at the output of the system (V_{BGD}) is then measured. The noise spectrum (E_n) of the device referred to its gate is obtained by dividing the noise at the output of the chain by the gain after quadratic subtraction of the background,

$$E_n(f) = \sqrt{\frac{\overline{V_{in}^2}}{\Delta f}} = \sqrt{\frac{V_{TOT}(f)^2 - V_{BGD}(f)^2}{G(f)^2}}. \qquad (7.12)$$

The DUT is biased with a power supply whose noise is negligible compared to the transistor noise to be measured. The DUT is placed in a metal box to shield it from outside noise sources.

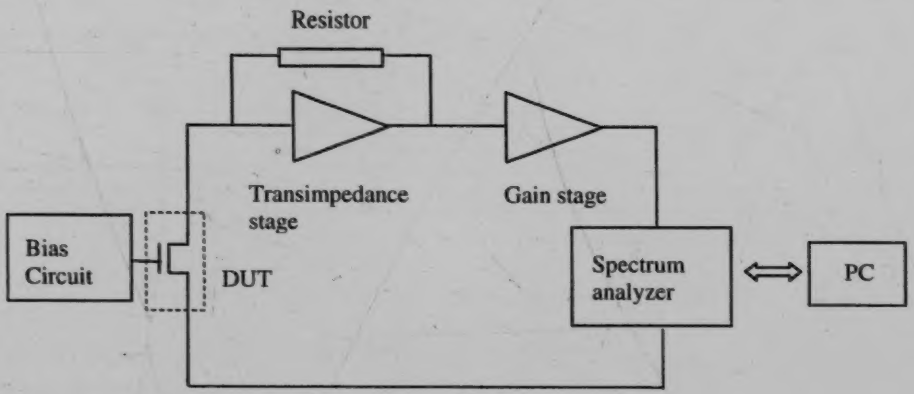


Figure 7.1: Schematic of noise measurement setup.

In order to measure the noise degradation, the devices are irradiated at room temperature with X-rays (maximum energy of 320 keV) produced by an irradiation system at the Centre of Subatomic Research, University of Alberta. More information about radiation procedure can be found in chapter 5.

7.2.3 Measurement results

The gain versus frequency data for each device under each gate voltage setup were measured and fitted to a fourth-degree polynomial expression, which is used in Equation 7.8 to calculate the final noise spectrum. Figure 7.2 shows an example of gain versus frequency for an enclosed-gate transistor in DUT0: $L = 1$ μm, $V_{gs} = 0.6$ V, $V_{ds} = 0.2$ V; the black curve is a plotted polynomial function fitted to the measured data.

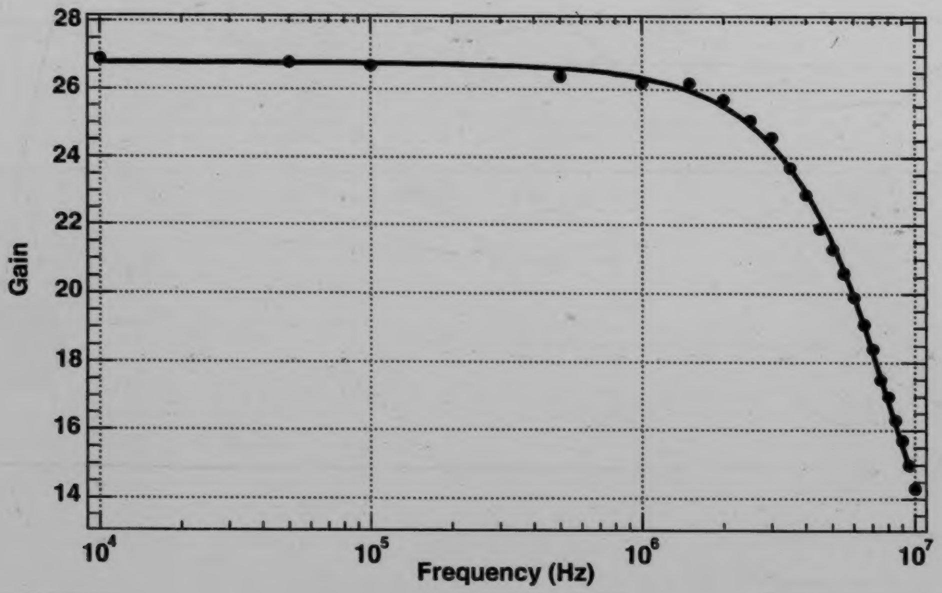


Figure 7.2: An example of gain versus frequency of an enclosed-gate transistor in DUT0: $L = 0.5$ μm, $W = 2.93$ μm, $V_{gs} = 0.6$ V, $V_{ds} = 0.2$ V.

Figure 7.3 shows an example of noise spectra measured from one ELT. The noise spectrum diagrams of the enclosed-gate transistor in DUT0, L = 1.0 μm, W = 3.95 μm, V_{gs} = 0.6 V, V_{ds} = 0.1 V, 0.2 V, 0.3 V, 0.4 V, 0.5 V, 0.6 V and 0.7 V, are shown in Figure 7.3.

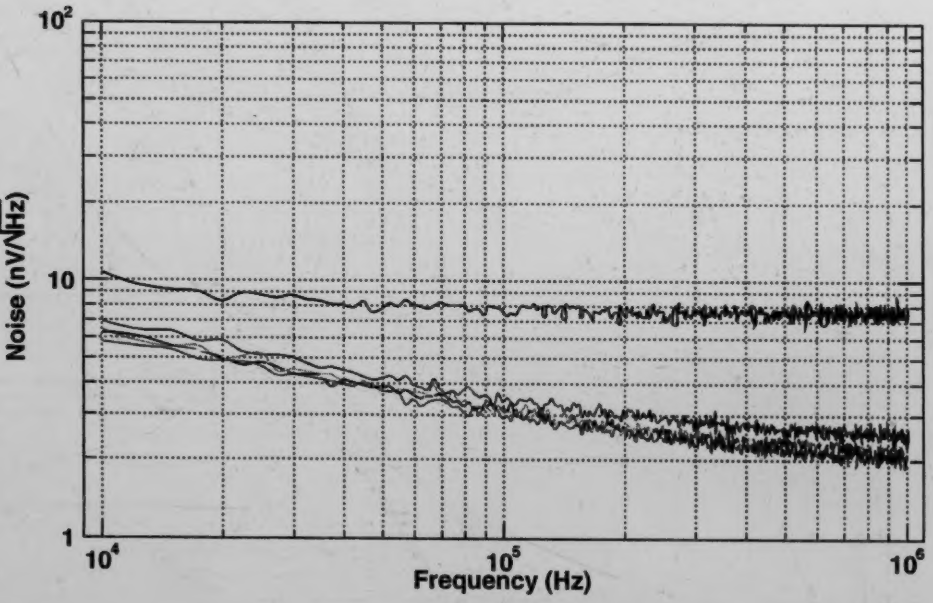


Figure 7.3: An example of noise versus frequency diagram of an enclosed-gate transistor in DUT0, L = 1 μm, W = 3.95 μm, V_{gs} = 0.6 V, V_{ds} = 0.1 V (black curve), 0.2 V (red curve), 0.3 V (green curve), 0.4 V (dark blue curve), 0.5 V (yellow curve), 0.6V (pink curve) and 0.7 V (light blue curve).

An example of a noise versus frequency diagram of an enclosed-gate transistor in DUT0, $L = 1$ μm, $W = 3.95$ μm, $V_{gs} = 0.6$ V, $V_{ds} = 0.1$ V, 0.7 V, before and after irradiation of 29 kGy(SiO_2), is shown in Figure 7.4. From the curves, one sees that the overall noise after irradiation changes only a limited amount. This small shift can also be observed in Table 7.1.

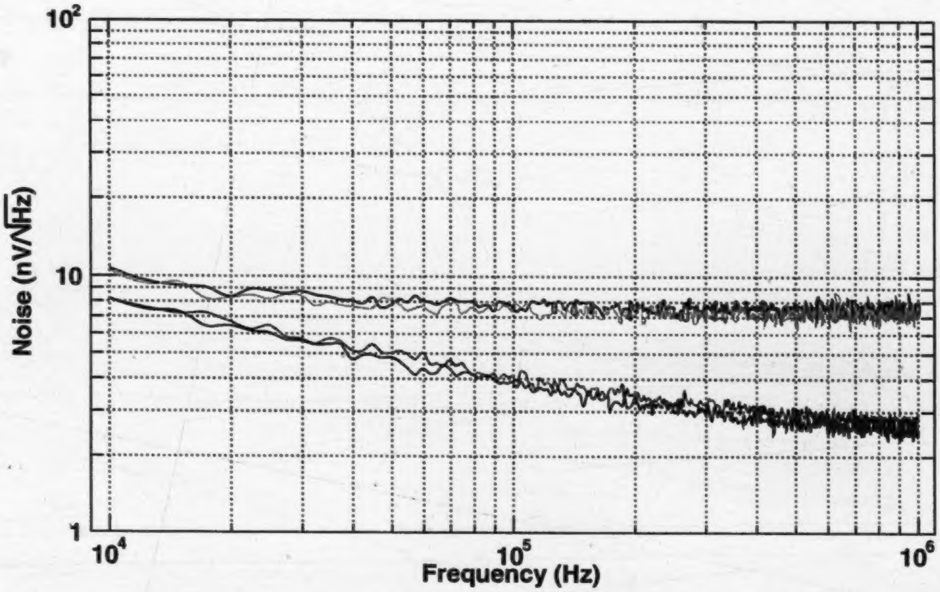


Figure 7.4: An example of a noise versus frequency diagram for an enclosed-gate transistor in DUT0, $L = 1$ μm, $W = 3.95$ μm, $V_{gs} = 0.6$ V, $V_{ds} = 0.1$ V (black and green curves), 0.7 V (red and blue curves), before (black and red curves) and after radiation (green and blue curves) of 29 kGy(SiO_2).

The channel thermal noise and K_a are extracted and listed in Table 7.1, for the enclosed-gate transistor of length is 1 μm in DUT0 with different drain voltages, before and after irradiation, where Vgs = 0.6 V. The channel thermal noise decreases with increasing drain current (increasing V_{ds}), and with the corresponding increase in transconductance. This trend supports the theory in Equation 7.6. From the table, one can also observe that the channel thermal noise also decreases after certain dose of radiation. However, the decreased amount does not exceed 10 per cent at 29 kGy(SiO_2) absorbed dose. The results are for one device, variation may be present during different devices.

V_{ds} (V)	Parameters	Pre- Radiation	Post-Radiation	Variation
0.1	Channel thermal noise ($nV/Hz^{0.5}$)	6.43±0.06	6.06±0.06	-0.29
	K_a (C^2/m^2) 10^{-27}	6.78±1.25	7.07±1.23	-0.37
0.2	Channel thermal noise ($nV/Hz^{0.5}$)	2.12±0.07	1.89±0.07	-0.23
	K_a (C^2/m^2) 10^{-27}	8.05±0.80	7.35±0.76	-0.70
0.3	Channel thermal noise ($nV/Hz^{0.5}$)	1.80±0.07	1.65±0.07	-0.15
	K_a (C^2/m^2) 10^{-27}	7.28±0.76	6.77±0.71	-0.51
0.4	Channel thermal noise ($nV/Hz^{0.5}$)	1.81±0.07	1.62±0.07	-0.19
	K_a (C^2/m^2) 10^{-27}	7.07±0.74	6.62±0.70	-0.45
0.5	Channel thermal noise ($nV/Hz^{0.5}$)	1.76±0.07	1.56±0.07	-0.20
	K_a (C^2/m^2) 10^{-27}	6.70±0.73	6.02±0.67	-0.68
0.6	Channel thermal noise ($nV/Hz^{0.5}$)	1.76±0.07	1.57±0.07	-0.19
	K_a (C^2/m^2) 10^{-27}	6.48±0.71	6.08±0.67	-0.40
0.7	Channel thermal noise ($V/Hz^{0.5}$)	1.73±0.07	1.56±0.07	-0.17
	K_a (C^2/m^2) 10^{-27}	6.58±0.71	6.20±0.69	-0.38

Table 7.1: Extracted channel thermal noise and K_a, from the enclosed-gate transistor of length is 1 μm in DUT0 with different drain voltages, before and after 29 kGy(SiO_2) absorbed dose irradiation, $V_{gs} = 0.6$ V.

Chapter 8 Configurable SRAM Macro Design to Resist Total Dose Effects

Many ASICs and system-on-chip (SOC) used in radiation environments require the use of rather large memories [Klo02, Fre98]. Using the special layout techniques (ELTs and guard rings), the memories can be designed to guarantee robustness against total dose effects over the lifetime of the chips. The lack of SRAM blocks and the absence of design automation tools for generating customized SRAM blocks that employ the radiation-tolerant layout rules are the primary motivation for the work presented in this chapter.

This chapter presents a size-configurable architecture for embedded SRAMs in radiation-tolerant, 0.18-μm CMOS, ASIC designs. A digital library is developed by systematically using ELTs and guard rings to reduce leakage currents. Physical layout data includes a memory cell array and abutted peripheral blocks: column address decoder, row address decoder, timing control logic, I/O circuitry and power lines. Some blocks are re-configurable to accommodate various word counts and bit capacities.

In the design, some low-power techniques were adopted [Ito95], such as address transition detection, divided word lines, and self-timing circuitry. The divided word line scheme [Yos83, Min84] is an effective way to reduce power consumption through the partial activation of multi-divided word lines. A dynamic divided word line (DDWL) scheme [SAK84], which combines a divided word line structure and an automatic power down (APD) scheme, is used in the design [Soo85]. In order to implement the APD function, a word line is activated dynamically by a pulse wider than the access time.

A test chip of a SRAM macro-cell has been designed, simulated and fabricated.

8.1 Memory architecture

The internal architecture of the SRAM design is shown in Figure 8.1. It consists of an array of static memory cells coupled with the necessary write and read logic, a global row decoder, a column decoder, a set of buffers for the addresses and the data input ports, latches for the data output ports, and self-timed logic circuitry controlling the operation of the SRAM macro-cell.

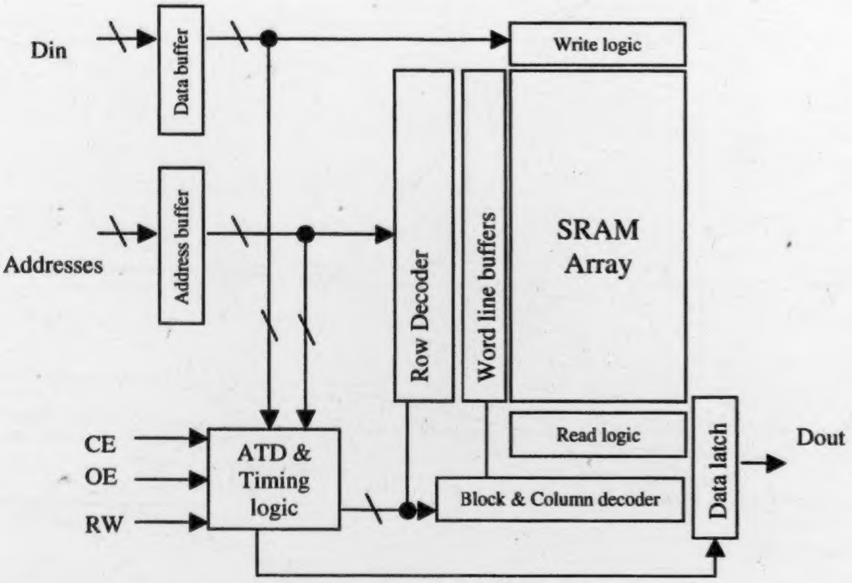


Figure 8.1: Block diagram of the SRAM architecture.

The cells in the memory array are accessed by the row decoder which selects the one word line, and by the column decoder which selects the appropriate bit lines. The row decoder has a fixed size of 128 word lines and uses the seven least significant bits of the addresses. The remaining addresses are routed to the column decoder and block decoders.

Generally, the advantages of a CMOS static RAM over a dynamic RAM lie in its higher speed. The disadvantages are larger cell sizes, and hence lower storage density. The proposed SRAM is asynchronous, meaning that there is no external clock signal for the proposed SRAM. An address transition detector (ATD) is incorporated in the SRAM to generate the activation pulse for the ATD function. This ATD also triggers equalization of bit lines (BLs) and sense lines (SLs) to prepare for a fast access time [Sak84].

8.2 Memory cell design

The memory cell is based on a conventional cross-coupled inverter design. The sizes of NMOS transistors are much larger than those of the PMOS in the inverters so that it is harder to write to the cells. In this way, the cell is more tolerant to single-event upset. The cells use PMOS transistors as access devices for ease of layout. All of the NMOS transistors are laid out with enclosed-gate transistors and are separated with guard rings. The size is 6.9 × 8.4 μm^2. The layout is shown in Figure 8.2.

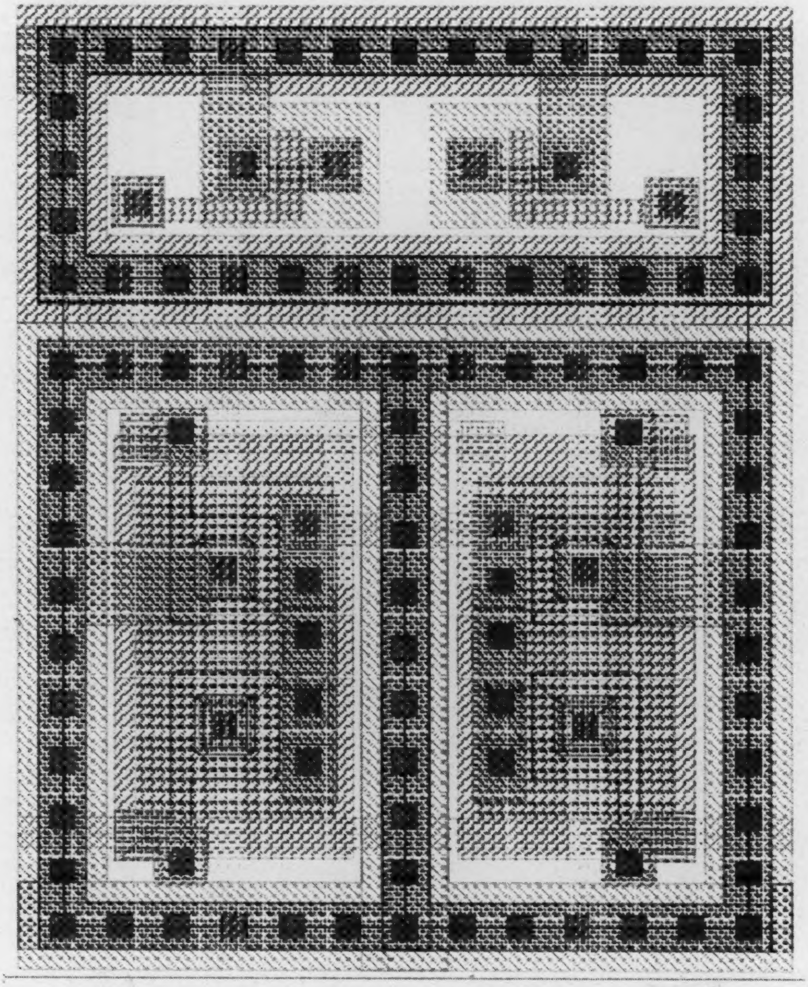
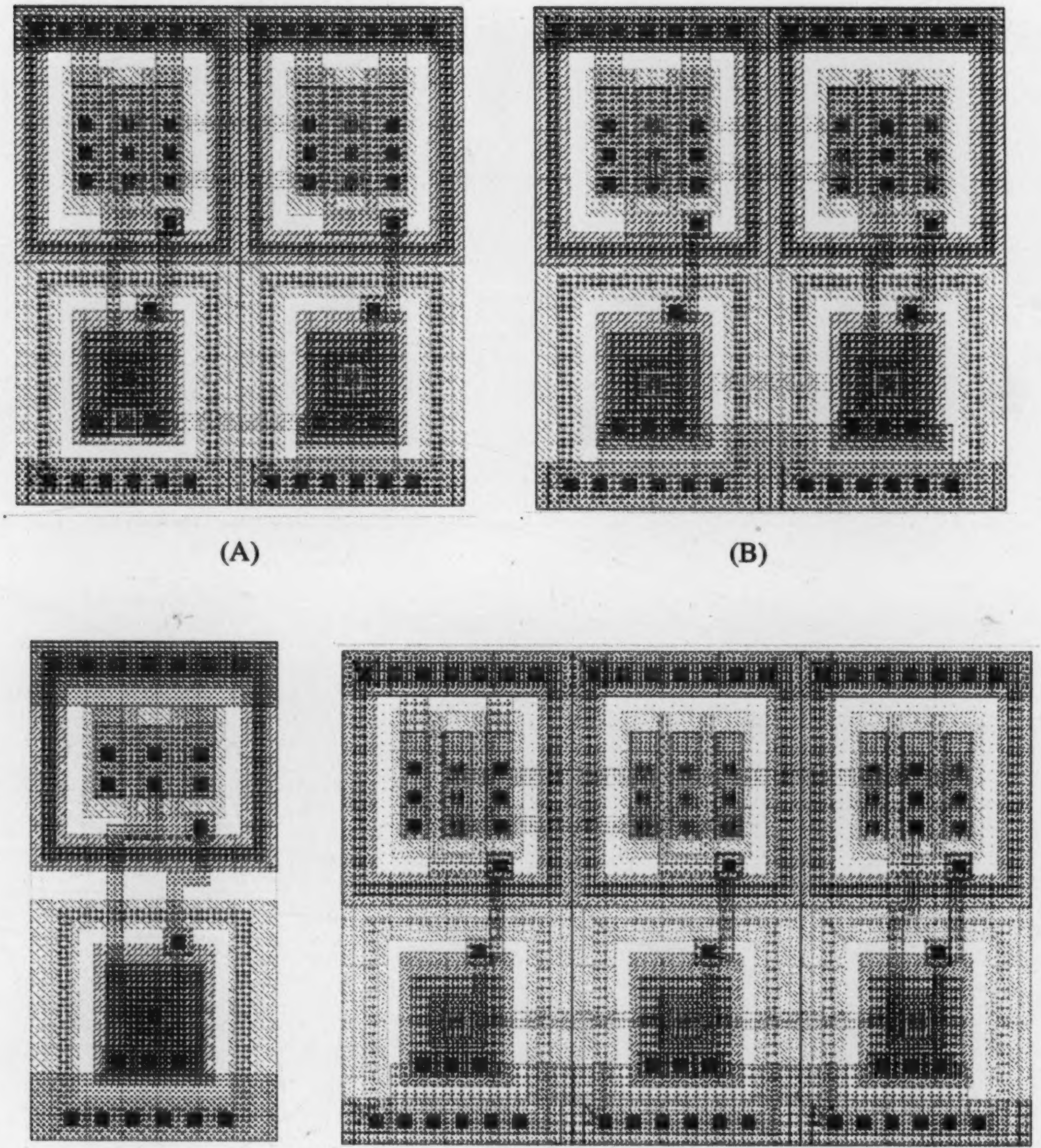


Figure 8.2: Layout of a SRAM cell with ELTs and guard rings.

8.3 A digital library with ELTs and guard rings

In order to systematically use NMOS ELTs in the SRAM, a digital library was developed. It includes the basic components for building the circuit. Various fan-outs of inverters and buffers are included in the library. Buffers include two or three stages of inverters with carefully sized transistors according to the different fan-outs. The library has 2-input and 3-input NOR, OR, NAND, AND, XOR gates with a fan-out of one. Various gate fan-outs were realized by using different buffer sizes to hasten the design process. D flip-flops and registers were also developed. The ratios of the NMOS and PMOS transistors were carefully designed so that the rising time and falling time are relatively equal. All the NMOS transistors were laid out with enclosed-gate transistors, and guard rings were systematically placed between devices with different potentials; N type guard rings were placed around PMOS transistors and P type guard rings were placed around NMOS transistors. Figure 8.3 shows the layouts of some gates developed, namely, an inverter with a fanout of one, a two-input NAND gate with a fanout of one, a two-input NOR gate with a fanout of one, and a three-input NOR gate with a fanout of one.

The area of the components using ELTs and guard ring in the library are generally 50 per cent larger than those of in the standard library.



(A) (B)

(C) (D)

Figure 8.3: (A) Layout of a two-input NAND gate with one fanout of one, (B) layout of a two-input NOR gate with a fanout of one, (C) layout of an inverter with a fanout of one, (D) layout of three-input NOR gate with a fanout of one.

8.4 Divided word line structure

The divided word line scheme was adopted to minimize power consumption. The word line has a hierarchical structure of two levels, namely global and local word lines [Yos83], as shown in Figure 8.4. Some of the addresses are decoded to activate the global word line and the remaining address lines are decoded by a block decoder to activate the vertical block enable lines. The local word line buffers receive the enable signals from the block decoder and drive the selected local word line in a selected block for read or write operation. Since the global word lines are not connected directly to memory cells, the capacitance of the global word line is relatively small, reducing the access time. The global word line is laid out by a metal layer, which also reduces the delay. Low power dissipation is expected because only one local word line is selected at a time, so only a small number of memory cells are activated. In the 1k × 9 bit test chip configuration, there are four 256 × 9 bit blocks, which will be activated only one at a time, so the current reduction compared to a conventional architecture is ¼. When a larger memory capacity is required, there are more blocks needed, and more power can be saved by using this structure.

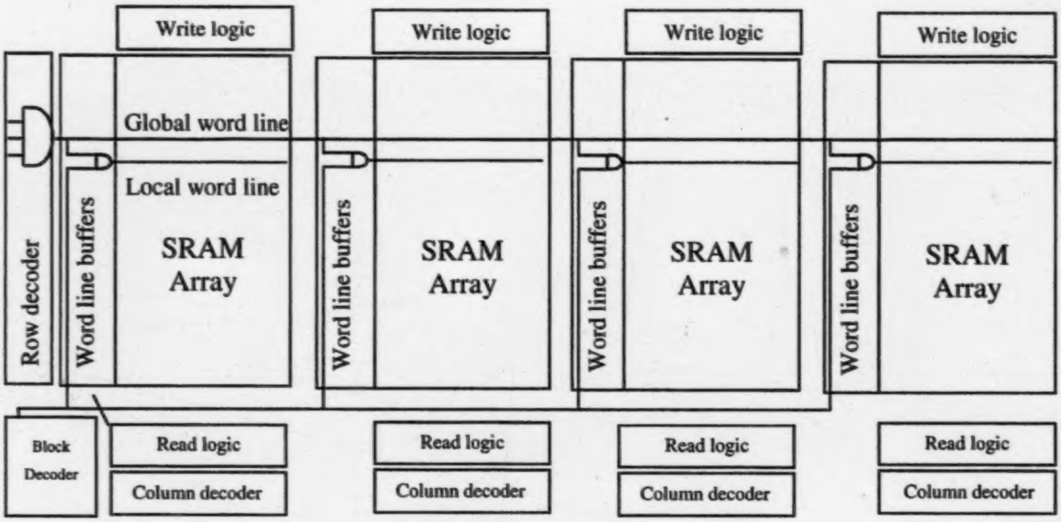


Figure 8.4: Block diagram of the divided word line structure.

8.5 Automatic power down function

When an address changes, the address transition detector creates two types of timing signals, namely, equalization clocks and activation clocks. The activation signals include sense amplifier activation clocks (ENSA and ENMA) and a word line activation clock (WLactive), which have a pulse width wider than the access time. The clock controlled word lines are one of the main features of the DDWL scheme. These activation signals control global and local word lines, two-stage sense amplifiers, so as to turn off all the DC paths after a read or write operation is over. Consequently, no DC power is consumed when the SRAM is in the idle state. This is the principle of the automatic power down function. A schematic of the core part and a rough sketch of internal waveforms are shown in Figure 8.5.

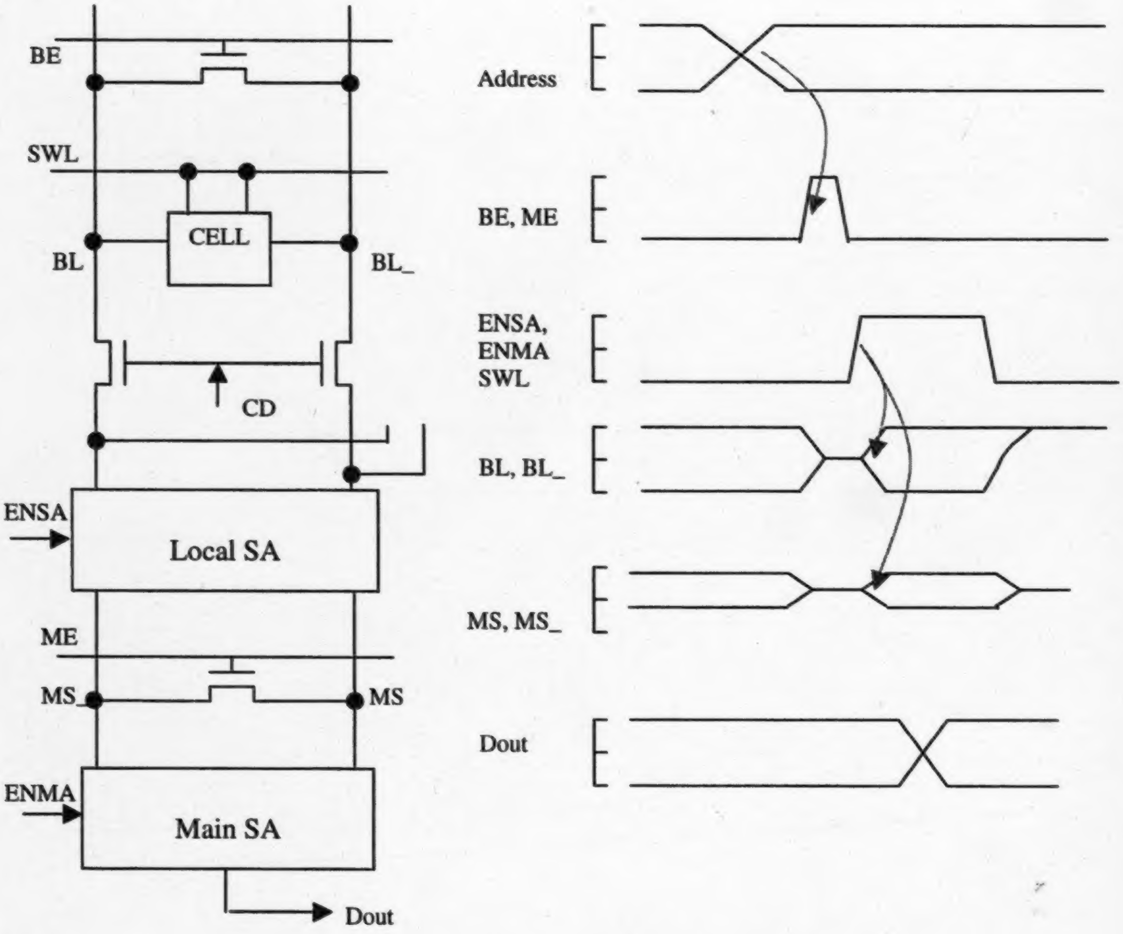


Figure 8.5: A schematic of the core part and a rough sketch of internal waveforms.

8.6 Sense amplifiers and equalization

There are two main types of sense amplifiers: latch-type and current mirror amplifiers. The latch-type is commonly used in dynamic RAMs because of its relatively small size and it is better able to fit into the narrower column pitches of dynamic RAMs. The disadvantage is that the timing of the latch clock is very critical. The latch timing should come after the slowest memory cell pushes out the stored information to the bit lines; otherwise, a malfunction could occur. On the other hand, it would also degrade the access time if the latch timing comes too late. The current mirror amplifiers are essentially static. There is no constraint on latch timing. Moreover, the relatively small voltage swing of the bit lines is indispensable for fast equalization and precharge. Based on these considerations, the current mirror sense amplifier approach is used in this design.

Corresponding to the divided word line scheme, a hierarchical structure is also adopted for sense lines, namely, bit lines and main sense lines. This double sense line structure reduces the capacitance of main lines so as to reduce the sensing delay.

A two-stage current-mirror sense amplifier is used to achieve fast sensing. The schematics are shown in Figure 8.6. The local sense amplifier senses the voltage differences between bit lines, and drives the differential main sense lines (MS, MS_). The main sense amplifier is used to sense the main sense lines.

The bit lines and sense lines are equalized and precharged by using equalization clocks (BE) and (ME) before information is read out from the memory cells. This is shown in Figure 8.5. The equalization is done in parallel with address pre-decoding, adding no extra delays to the sensing operation. In fact, it reduces the access time because considerable time is required to cancel the effect of previous data if there is no equalization.

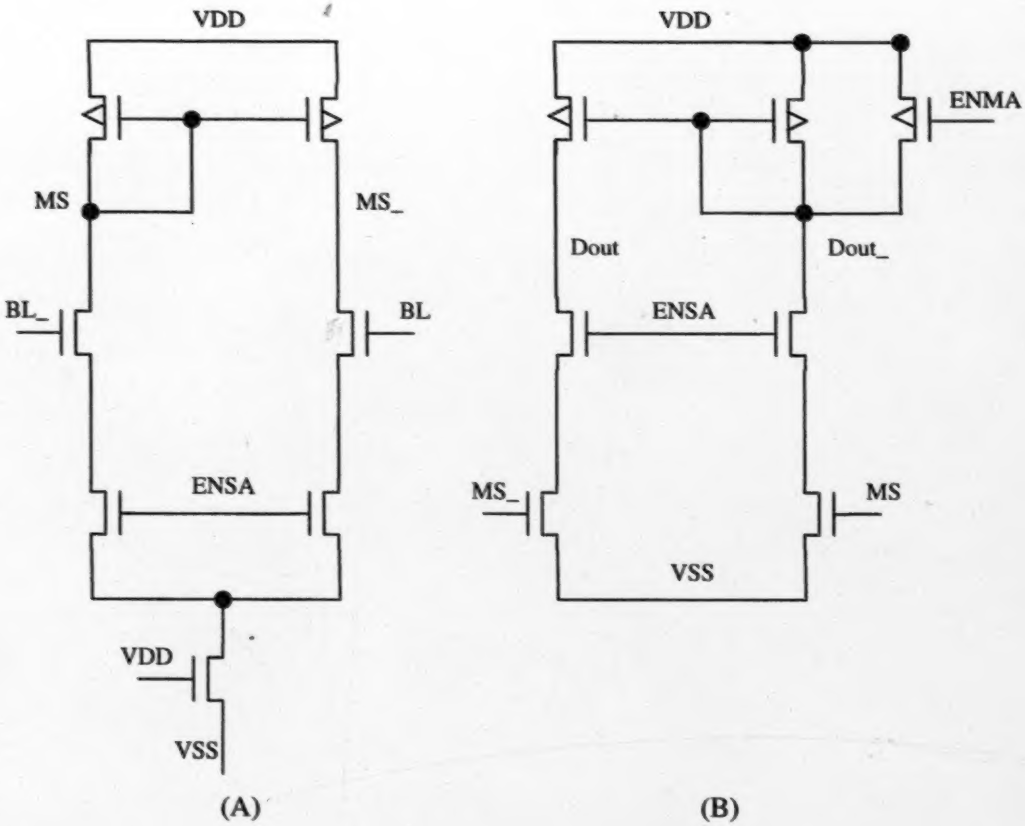


Figure 8.6: (A) The schematic of the local current mirror sense amplifier; (B) the schematic of main current mirror sense amplifier.

8.7 Performance and other features

A 1k-word-deep by 9-bit-wide word SRAM test chip was designed and fabricated. The layout is shown in Figure 8.7. The memory array consists of four 256 × 9 bit blocks.

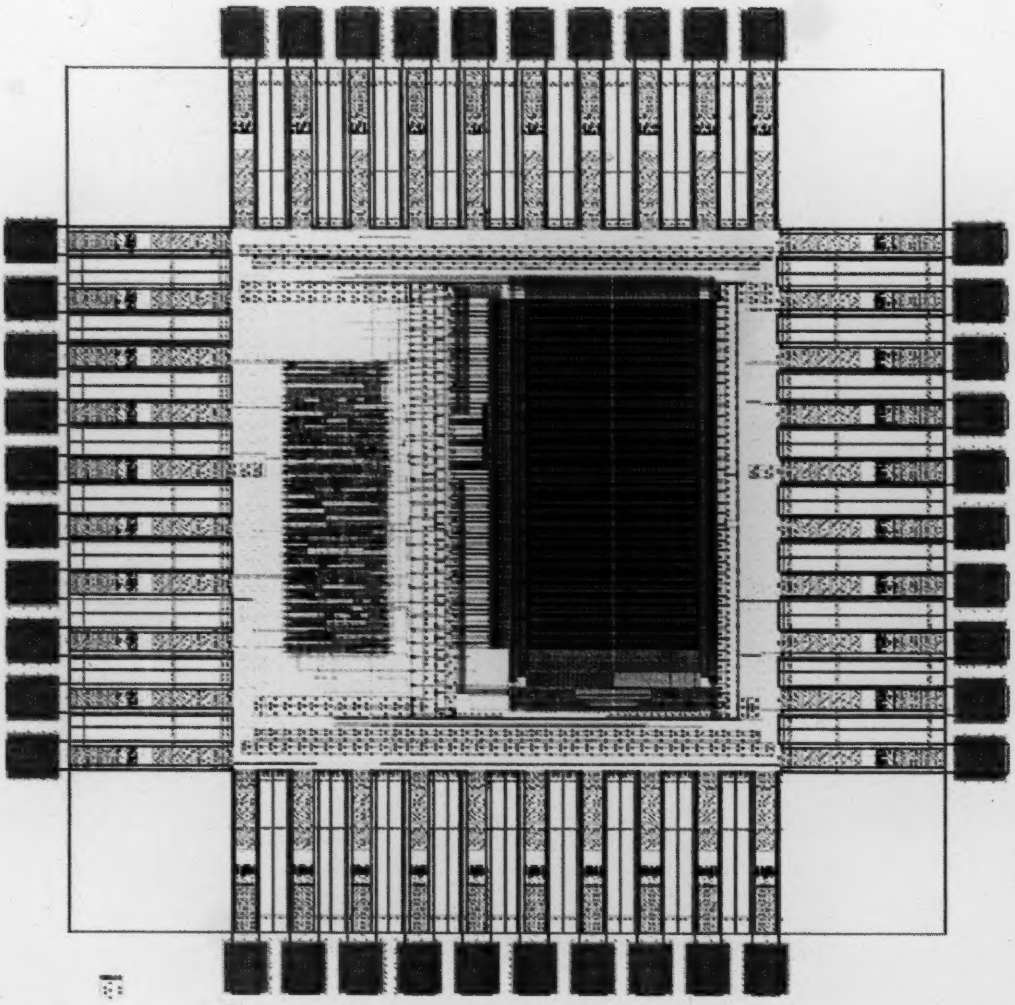


Figure 8.7: Layout of the 1k × 9 bit SRAM test chip. The right part in the core is the memory arrays and row/column decoders; the left part is the peripheral circuits of the memory.

The internal timing of the SRAM macro cell is completely asynchronous and self-timed. The timing logic uses a combination of hand shaking and address transition detection to realize internal timing loops. Figure 8.8 shows the timing diagram for a write followed by a read operation.

To write into the cell, data are placed on the BL and BL_ lines by the appropriate write signal (WE0). Then the selected word line is activated (SWL0). This forces the appropriate memory cell to flip into the state represented on the bit lines. During the writing operation, the two stages of sense amplifiers are also enabled by (ENSA) and (ENMA) to output the bit line data to the output data bus so as to update the output bus according to the new address.

A read is performed by generating a short pulse of equalization signal (SBE), to equalize the bit lines and sense lines. This will set both BL and BL_ to high. During this time, the row decoder is decoding the addresses at the same time. After the equalization signal is low again, the desired local word line (SWL0) is selected with the combination of the appropriate block select signals. The local sense amplifier (ENSA) and the main sense amplifier (ENMA) are also enabled. At this time, the data in the selected cell will pull either the BL or BL_ line to low and be amplified at local and main amplifiers.

Some typical characteristics of the SRAM are listed below in table 8.1. The timing parameters were obtained from simulation.

Organization	1k x 9 bit
Process	0.18-μm CMOS
Supply voltage	1.8 V
Address access time	8 ns
Chip select access time	8.4 ns
Chip size	1.5 x1.5 mm^2
Cell size	6.9 x 8.4 μm^2

Table 8.1: Some characteristics for the SRAM. The timing parameters are measured from simulation.

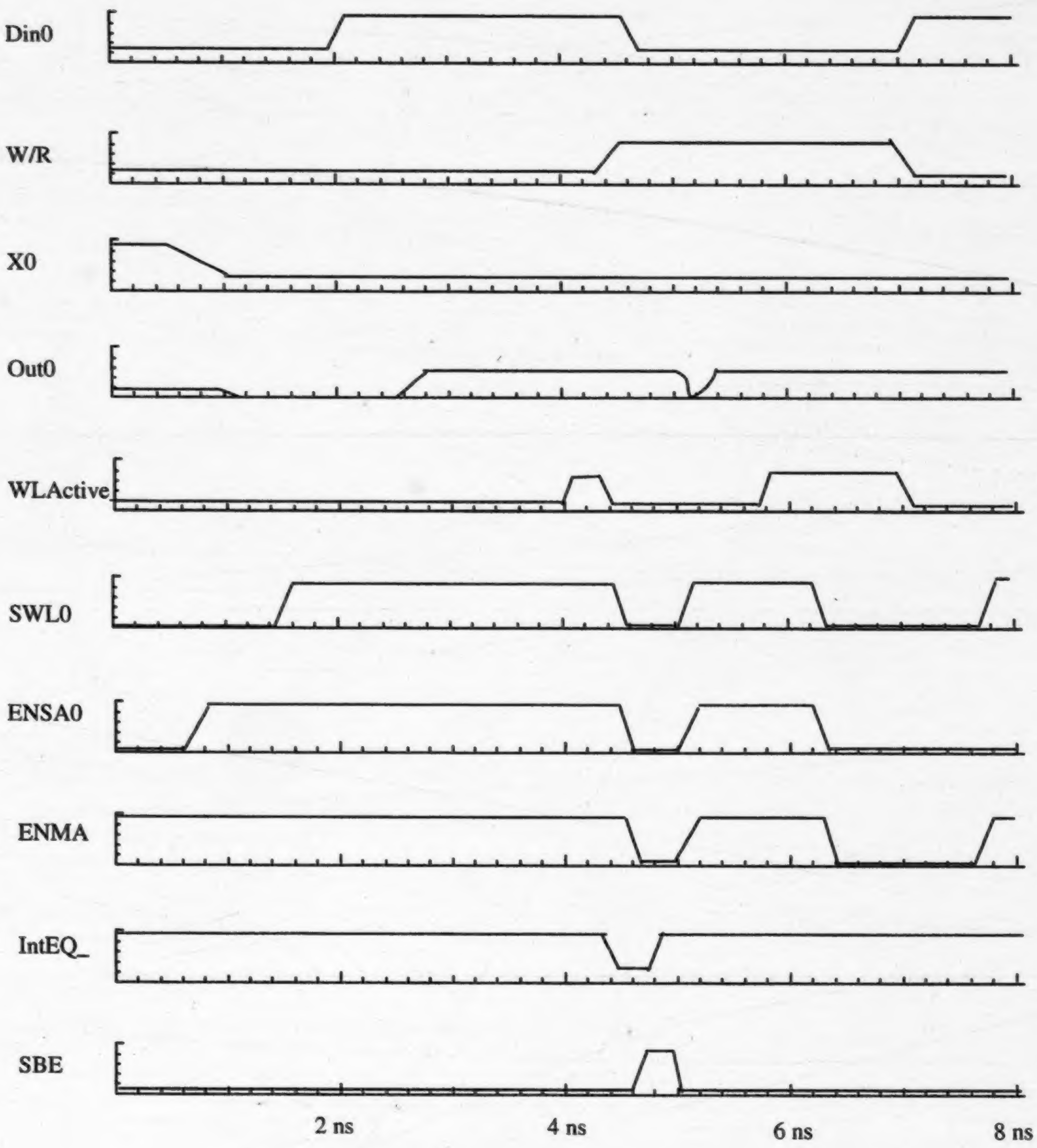


Figure 8.8: The timing diagram for a write followed by a read operation.

Chapter 9 SRAM Design to Guard Again Single-Event Effects

This chapter presents an investigation of an SRAM design to guard again SEU using a 0.18-µm commercial CMOS technology to reduce costs and improve performance. As shown in previous chapters, total dose effects and single-event latch-up are less significant and can be prevented by systematically using guard rings and edgeless devices. On the other hand, SEU becomes more significant in deep submicron technologies than older ones because of the decreased critical charge, as discussed in chapter 3. Many strategies based on circuit design approaches have been introduced to harden microelectronic circuits against the SEU in micron technologies. They need to be fully evaluated with deep submicron technologies and an optimal approach is to be introduced.

9.1 SRAM hardening techniques

There are many techniques to hardening the SRAM to guard against SEU. Two common solutions are: using enhanced critical charge hardening techniques and redundant circuit hardening techniques. These two solutions are studied and compared in the following sections.

9.1.1 SRAMs using enhanced critical charge hardening techniques

The enhanced critical charge hardening technique includes increasing the transistor drive, capacitive hardening and resistive hardening.

High drive transistors can quickly remove/replace SEU injected charge, shortening the time duration of the disturbance. Large high drive transistors also have increased node capacitance, which reduces the voltage excursions caused by the SEU injected charge [Whi93]. Increasing the capacitance of critical nodes to reduce the voltage change due to SEU injected charge is the basic concept behind the capacitive hardening of circuits. Power is consumed when charging/discharging circuit capacitance each time the logic level of a node changes. Increasing circuit capacitance due to high drive transistors or other capacitive hardening methods also increases the dynamic power consumption of the circuit. Designing a cell to reject short duration signals places a constraint on the maximum speed at which the circuit can operate. With the decreasing feature size, i.e. in deep submicron technologies, node capacitance also decreases. With the increasing sizes of NMOS transistors, the SRAM cell is more difficult to write and makes the cell more hardened. The simulation result is discussed in the next section.

Resistive hardening involves the use of resistors in the memory element feedback paths, to create, in conjunction with the gate capacitance, a low pass filter to reject the effects of SEU while passing the longer duration legitimate signals [Die82]. The schematic is shown in Figure 4.5. The feature size assumed in [Die82] is 2 μm. According to the design of [Die82], it is possible to design an RC filter to reject SEUs and still allow the circuit to operate at hundreds of megahertz. The resistances required to provide SEU immunity are typically 100 kΩ to 1 MΩ, requiring high resistivity polysilicon in order to keep the resistor elements small. The disadvantage is that the approach is subject to wide resistance variations across a generally accepted variation in commercial processing parameters. This problem is further exacerbated by a very large negative temperature coefficient.

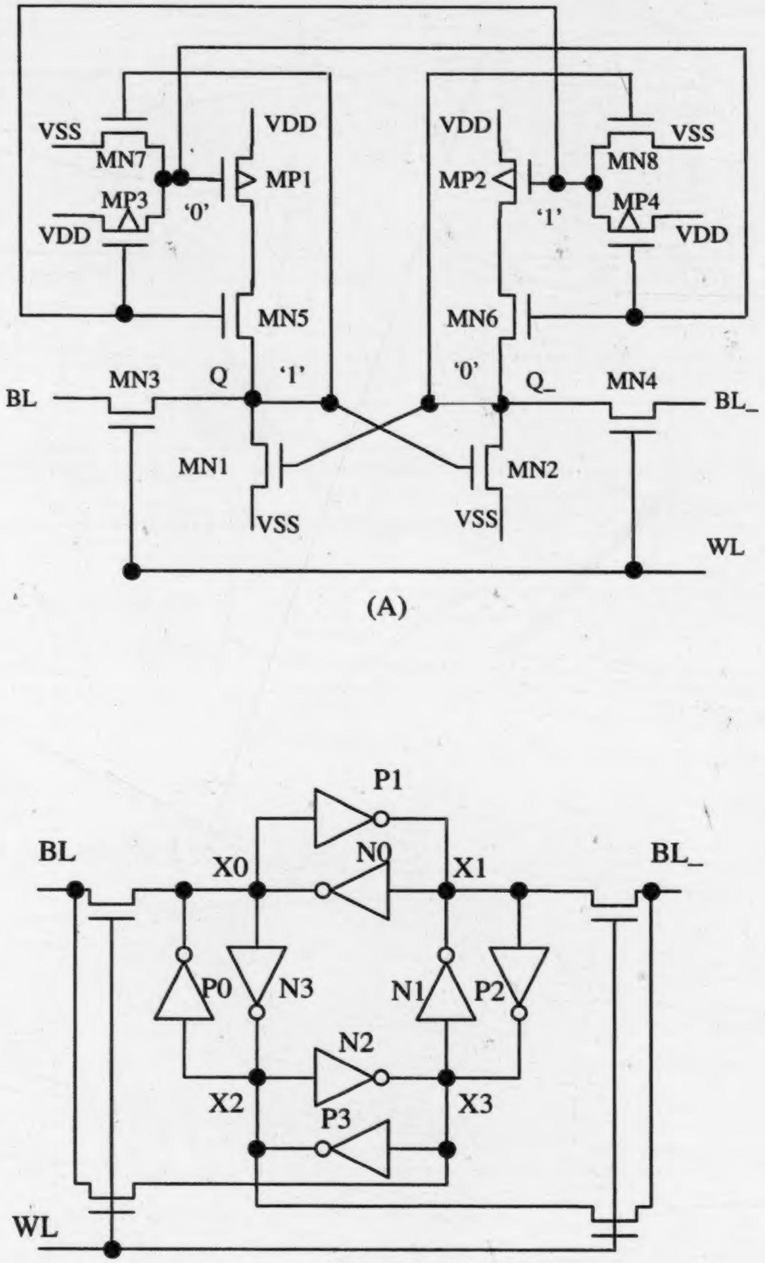
With the decreasing feature size of the deep submicron technologies, the gate capacitance of transistors decreases. It can be predicted that the resistances required of the poly-resistor will increase. Such a cell was laid out using 0.18-μm technology. The cell performance was studied and simulated with HSPICE in Cadence. The results are discussed in the next section and compared with those of other techniques.

9.1.2 SRAMs using redundant circuit hardening techniques

Two fundamental concepts are used to design SEU immune storage cells using conventional CMOS process. First, redundancy in the memory circuit maintains a source of uncorrupted data after a SEU. Second, data in the uncorrupted section provides specific "state restoring" feedback to recover the corrupted data.

There are two types of storage cell designs that implement these principles. The first type combines the three main techniques for upset hardening: the use of NMOS or PMOS redundant latches, the use of single-transistor feedback loops to obtain state-dependent active feedback circuits, and the use of ratioed inverters to avoid transient pulse propagation. The typical cell of this type is called a heavy ion tolerant (HIT) cell [Vel94]. The schematic is shown in Figure 9.1A. Testing showed that the hardened HIT cell design is less sensitive to upsets at least by a factor of 10 than the standard cell design [Vel 94]. The drawbacks of this kind of storage cell are: high area overhead, high power dissipation and critical ratioed transistors sizing in order to achieve upset immunity. This storage cell introduced in [Vel94] was simulated and fabricated in a 1.2-μm technology. It is necessary to evaluate its performance in deep submicron process. This storage cell was laid out with 0.18-μm technology. The ratios of different size transistors were determined by Cadence simulation. Its performance was studied by HSPICE simulation. The results are listed and compared with those of other techniques in the next section.

The second type of storage cell is called the Dual Interlocked Storage Cell (DICE) [Cal96], which used a novel 4-node redundant structure. The schematic is shown in Figure 9.1B. The transistors can be scaled to the minimum size, and there is no direct DC path in the cell. So the power and area may be smaller than the other cell types. There is no single sensitive node in the circuit. This means that only when two nodes are affected simultaneously will an upset occur. This cell was laid out with 0.18-μm technology. Its performance was studied and evaluated by HSPICE simulation. The simulation results are shown and compared with those of other techniques in the next section.



(A)

(B)

Figure 9.1: (A) Schematic of a HIT SRAM cell; (B) Schematic of a DICE SRAM cell.

9.2 Simulation results and discussions

The simulation technique involved the use of a trapezoidal, pulsed current source to emulate the subnanosecond dynamics of prompt charge collection at sensitive latch nodes. All simulations were run with nominal device parameters, minimum supply voltage levels and at specified temperatures. In this way, the response of the circuit to a single-event upset could be evaluated and the minimum amount of excess charge collected by the sensitive latch node needed to cause an upset could be ascertained. The current pulses are described with full width at half maximum, FWHM = 0.1 ns with its amplitude (I_{ampl}) adjusted to determine the critical charge for upset (Q_{crit}). The total charge deposited on the sensitive latch node is then simply

$$Q_{coll} = 0.1\times10^{-9}\cdot I_{ampl} \,, \tag{9.1}$$

where the unit for Q_{coll} is pC, I_{ampl} is mA. This equation will be used for all the calculations of critical charge. All the simulations are performed at room temperature.

9.2.1 Enhanced critical charge hardening techniques

This technique can be realized by increasing the size of the NMOS transistors in a SRAM cell. The simulation was performed using HSPICE in Cadence. Table 9.1 shows the NMOS transistor width versus the critical charge.

NMOS transistors width (nm)	**Critical charge (pC)**
220	0.0142
660	0.0328
8000	0.4

Table 9.1: Width versus critical charge of the NMOS transistors in a SRAM cell.

From the Figure 9.2, one notices that the critical charge is directly proportional to the size of the NMOS transistors in the SRAM cell. This relationship is described by the following equation:

$$Q_{crit} = C_s \cdot \Delta V_{crit}, \tag{9.2}$$

where Q_{crit} is the critical charge, C_s is the storage capacitance, and ΔV_{crit} is the largest swing which can be operated without losing the stored information.

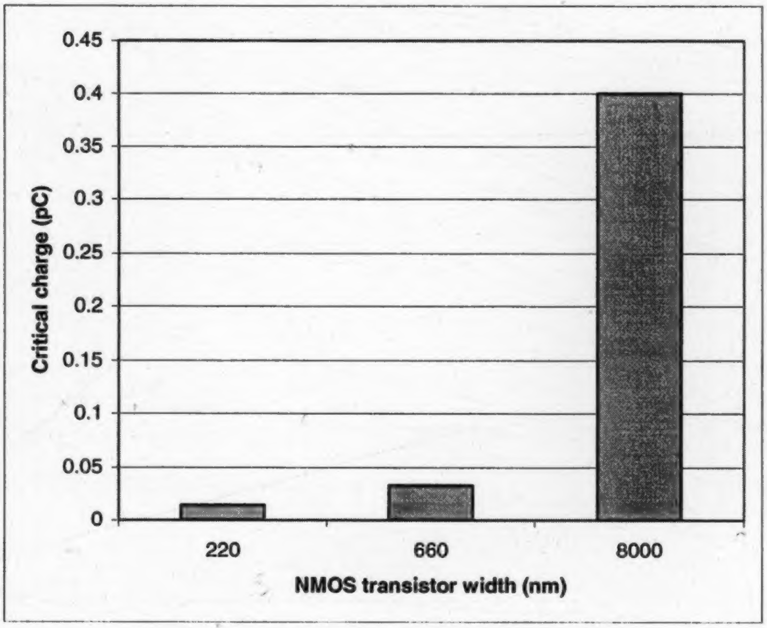


Figure 9.2: NMOS transistors width versus critical charge in a SRAM cell.

The maximum amount of charge that can be collected at a node does not exceed 3.0 pC for many radiation-hardened CMOS techniques [Hen87]. With this technique, the critical charge obtained (0.4 pC) is far less than this amount even if the size is very large (8.0 µm for a 0.18-µm process). So it is not applicable to the cases that SEUs are caused by heavy ions, which normally can cause huge charge collection in a node.

9.2.2 Redundant circuit hardening techniques

The HIT, DICE and resistor-hardened cells have been developed and laid out in Cadence to investigate their performance. Table 9.2 shows the size of each transistor in a HIT cell, as each transistor has to be carefully sized to make the cell function properly. A standard SRAM cell with the minimum size transistors was also developed and analyzed as a base case to compare with the other cells. These four types of SRAM cells were simulated with HSPICE in Cadence, and compared with respect to their electrical characteristics, such as critical charge, power, read time, write time and area in order to evaluate their performance.

NMOS	W (μm)	L (μm)	PMOS	W (μm)	L (μm)
MN1	0.61	0.18	MP1	1.2	0.18
MN2	0.61	0.18	MP2	1.2	0.18
MN3	1.05	0.18	MP3	0.51	0.18
MN4	1.05	0.18	MP4	0.51	0.18
MN5	0.61	0.18			
MN6	0.61	0.18			
MN7	0.82	0.18			
MN8	0.82	0.18			

Table 9.2: Transistor sizes for the HIT cell.

The power simulation technique involved the use of a resistor whose resistance can be neglected. SRAM cells are connected to a power supply through the resistor. The power is calculated through the current waveforms passing through the resistor in a complete write-read cycle, which includes operations of read, write and pre-charge. Then the power consumed at 100 MHz can be calculated. Power includes static and dynamic powers. Static power is obtained from the static part of current waveforms and the dynamic power is calculated from the pulses of the current waveforms. The charge in the pulses was calculated and converted to current so that the dynamic power could be obtained.

The write and read times provide a good measure of the functional response of the circuit. The write time is the time interval defined from the midpoint of the rising edge of an activated word line pulse to the midpoint of the rising edge of the feed-forward response of the latch node. The read time is the time interval defined from the midpoint of the rising edge of an activated word line pulse to the midpoint of the rising edge of the bit line. Area is measured directly from the layout of the cells. Table 9.3 lists the parameters for cells measured from simulations. STD-cell is a SRAM cell with minimum sizes. RES-cell is referred to as a SRAM cell designed in resistor-hardening techniques.

Cell type	**Write time (ns)**	**Read time (ns)**	**Q_{crit} (pC)**	**Area (μm^2)**	**Power (μW)**
STD	1.26	2.47	0.013	21	0.024
RES	3.01	2.37	>5	75	0.084
HIT	1.71	1.73	>5	68	0.31
DICE	1.03	1.93	>5	33	0.046

Table 9.3: Parameters for each studied cell.

From the Table 9.3, it can be noticed that all of the three hardened cells have very high critical charge (more than 5 pC). The write time of the DICE cell is the smallest among all of the studied cells. Its read time is only slightly larger than HIT cell. Its area has 50 per cent overhead compared to the standard cell, but is much smaller than other hardened cells. Its power is almost twice larger than the standard cell, but is much smaller than other hardened cells. One can conclude that DICE cell has overall better performance than other hardened cells.

Conclusions

During the last decade, vendors of radiation-hardened semiconductor technologies have faced a considerable reduction in the military market. The space community has focused its interest more on the use of Commercial-Off-The-Shelf (COTS) components rather than the highly expensive and less advanced components that they traditionally used in the past. As a consequence of this evolution, several semiconductor companies have abandoned the radiation-hard electronics market and now only a handful of companies in the world offer radiation-hard technologies suitable for radiation-hardened ASICs. Therefore, an alternative approach based on radiation-tolerant design techniques in a deep submicron CMOS technology has been investigated by the European Organization for Nuclear Research. Using a 0.25-μm technology and a layout approach (ELTs and guard rings) has proven to be an effective way to resist total dose effects.

This thesis confirms that the 0.18-μm CMOS technology (gate oxide thickness of 4.3 nm), combined with ELTs and guard rings, can effectively resist total dose effects to a very high level. The possibility of using such an approach fits well with the natural trend of CMOS technologies, which have been continuously scaling down. The thin gate oxides of submicron technologies are indeed inherently more radiation-tolerant than the thicker oxides present in less advanced technologies. Using a commercial deep submicron technology to build up radiation-hardened circuits introduces several other advantages compared to a dedicated radiation-hard technology. These are:

- State of the art technology (density, speed, many interconnection layers),
- Reduced power consumption,
- High yield and reliability,
- Low cost.

Other beneficial effects brought about by scaling down a technology include reducing the sensitivity to single-event latch-up and improving the general performance of the transistors.

On the other hand, a further scaling down of CMOS technologies could introduce new problems. Single-event upset sensitivity increases with the scaling down of a technology. Memory cells and logic are more easily disrupted by radiation. A further reduction of the power supply voltage, for example, can have an influence on the dynamic range, which in turn, reduces the noise margin for digital circuits. Moreover, deep submicron transistors introduce more effects (hot carrier effects, short channel effects), which need more modeling efforts, as well as new CAD tools to comply with the increased design complexity.

After reviewing the advantages and disadvantages brought about by scaling down, the research contributions of this work can be described as follows. The main contribution of this thesis is the development and confirmation of a radiation-tolerant layout approach with 0.18-µm technology. To make extensive use of ELTs and guard rings to design ASICs for radiation environment applications in a deep submicron technology, a certain number of issues had to be investigated.

In chapter 5, some modeling issues were studied in order to utilize an enclosed geometry instead of a standard rectangular geometry. In particular, the modeling of the aspect ratio was evaluated and the asymmetries related to the ELTs (e.g., the output conductance) were also studied. In chapter 6, radiation tests were done on the ELTs with 0.18-µm technology to prove the effectiveness of the ELT and guard rings approach. The threshold voltage, leakage current, transconductance and subthreshold slope were extracted. A very limited degradation was noticed after absorption of 70 kGy(SiO_2) dose. Noise is also a crucial parameter for analog designers, and in particular is very important for the front-end circuit of a particle detector. A study was performed by an evaluation of the noise performance of the 0.18-µm technology (chapter 7). An investigation was conducted into the effects of the transistor inversion conditions and irradiation on noise levels up to a total dose of 50 kGy(SiO_2). The noise shift induced by radiation was less than 10 per cent for one device. The results pave the way for analog applications using ELTs with 0.18-µm CMOS technology.

With the knowledge developed in chapters 5, 6 and 7, more complex circuits can be designed. A digital library was developed using ELTs and guard rings to reduce the leakage current. A configurable SRAM architecture was introduced in chapter 8. Some low-power design approaches were adopted. A 1k × 9 bit SRAM test chip was designed, simulated and fabricated. Single-event upsets are expected to become more serious for memory in radiation environments with the use of scaled down technologies. SRAM cell hardening techniques were studied and evaluated in chapter 9, and the best solution with the current technology was presented.

To conclude this thesis, I would like to make one final point. FPGAs have become more and more popular in digital design because of their flexibility. The demand for radiation-hardened FPGA has also increased in both the space and military communities. The layout approach presented in this thesis can easily be used in FPGA architectures by developing a digital library with ELTs and guard rings. In this way, tolerance to total dose effects in FPGAs can be enhanced using commercial deep submicron technologies. Moreover, the configurable SRAM (or SRAM generator) with ELTs and guard rings can also be easily embedded into the FPGA. In this way, it opens a new area for radiation-hard FPGA design.

Bibliography

[Abi86] A. A. Abidi, “High-Frequency Noise Measurements on FETs with Small Dimensions”, *IEEE Transactions on Electron Devices*, vol. 33, no. 11, pp. 1801-1805, November 1986.

[Ale96] D. R. Alexander, “Design issues for radiation tolerant microcircuits for space”, *Notes of the Short Course of the IEEE Nuclear and Space Radiation Effects Conference*, Indian Wells (California), July 1996, Section V.

[All94] M. Allenspach, J. R. Brews, I. Mouret *et al.*, “Evaluation of SEGR threshold in power MosFets”, *IEEE Transactions on Nuclear Science*, vol. 41, no. 6, December 1994, pp. 2160-2166.

[Ane97] G. Anelli, M. Campbell, C. Dachs *et al.*, “Total Dose behaviour of submicron and deep submicron CMOS technologies”, *Proceedings of the Third Workshop on Electronics for LHC Experiments* (LEB97, London, England, September1997), pp. 139-143.

[Ane99] G. Anelli, M. Campbell, M. Delmastro *et al.*, “Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects”, presented at the IEEE Nuclear and Space Radiation Effects Conference (NSREC ’99, Norfolk, Virginia, USA, July 1999), *IEEE Transactions on Nuclear Science*, vol. 46, no. 6, December 1999, pp. 1690-1696.

[Ane99a] G. Anelli, “Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies”, 2000, Ph.D thesis.

[ATL] ATLAS public website: http://atlas.web.cern.ch/Atlas/Welcome.html.

[Bac84] G. Baccarani, M. R. Wordeman and R. H. Dennard, "Generalized Scaling Theory and its Application to a ¼ Micrometer MOSFET Design", *IEEE Transactions on Electron Devices*, vol. 31, no. 4, April 1984, pp. 452-462.

[Bea95] J. Beaucour, "Effects des rayonnements sur les composants électroniques: aspects fondamentaux", Notes of the Short Course of the 3nd European Conference on Radiation and its Effects on Components and Systems, Arcachon (France), September 1995, Short Course 1, second part, pp. 43-59.

[Bel99] A. A. Belyaev, A. E. Belyaev, *et al.*, "Effect of Microwave Radiation on the Physicochemical Properties of Some Semiconductor Materials (GaAs, GaP, InP) and Heterostructures, as well as on the Parameters of Surface-Barrier Diode Structures", *Semiconductor Conference, CAS '99 Proceedings, 1999 International,* Vol: 1, 5-9 Oct. 1999, pp. 385 – 388.

[Bes94] D. Bessot, R. Velazco, "Design of SEU-hardened CMOS memory cells: the HIT cell", *Proceedings of the 2nd European Conference on Radiation Effects on Devices and Systems* (RADECS 93, St. Malo, France, 13-16 September 1993), pp. 563-570.

[Bre80] J. R. Brews, W. Fichtner, E. H. Nicollian and S. M. Sze, "Generalized Guide for MOSFET Miniaturization", *IEEE Electron Device Letters*, vol. 1, no. 1, January 1980, pp. 2-3.

[Bru69] J. S. Brugler and P. G. A. Jespers, "Charge pumping in MOS devices," *IEEE Trans. Electron Devices,* vol. ED-16, p. 297, 1969.

[BSIM97] Y. Cheng *et al*, "BSIM3v3 Manual", *University of California*, Berkeley, 1996. On line http://rely.eece.berkeley.edu/

[Cal96] T. Calin, M. Nicolaidis, R. Velazco, "Upset Hardened Memory Design for Submicron CMOS Technology", *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, December 1996, pp. 2874-2878.

[Cam88] F. J. Campbell, "Fundamentals-radiation effects on electrical insulation", Electrical Insulation Magazine, IEEE, Vol. 4, Issue: 6, Nov.-Dec. 1988, pp. 30 – 34.

[Cam99] M. Campbell, G. Anelli, M. Burns *et al.*, "A pixel readout chip for 10-30 Mrad in standard 0.25 μm CMOS", *IEEE Transactions on Nuclear Science*, vol. 46, no. 3, June 1999, pp. 156-160.

[Can91] J. Canaris, "An SEU immune logic family", *Proceedings of the third NASA symposium on VLSI design*, Moscow, Idaho, USA, October 1991, pp. 2.3.1-2.3.12.

[CER] CERN, "Tutorials on Radiation Effects", *ATLAS Radiation Hard Electronics Web Page*, the content can be found at the URL: http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm#Tutorials

[Cha80] P. K. Chatterjee, W. R. Hunter, T. C. Holloway and Y. T. Lin, "The Impact of Scaling Laws on the Choice of n-Channel or p-Channel for MOS VLSI", *IEEE Electron Device Letters*, vol. 1, no. 10, October 1980, pp. 220-223.

[Cha91] Z.Y. Chang and W.M.C. Sansen, "Low-noise wide-band amplifiers in bipolar and CMOS technologies", Kluwer Academic Publishers, 1991.

[Cit99] S. Cittolin, "LHC experiments: Data Communication and Data Processing systems", presentation given at the 1999 CERN School of Computing, 12-

25 September 1999. See the URL:
http://cmsdoc.cern.ch/cms/TRIDAS/distribution/3.Misc/talks/CSC99.pdf

[Cri99] D. L. Critchlow, "MOSFET Scaling – The Driver of VLSI Technology", *Proceedings of the IEEE*, vol. 87, no. 4, April 1999, pp. 659-667.

[Dav95] B. Davari, R. H. Dennard and G. G. Shahidi, "CMOS Scaling for High Performance and Low Power – The Next Ten Years", *Proceedings of the IEEE*, vol. 83, no. 4, April 1995, pp. 595-606.

[Den74] R. H. Dennard, F. H. Gaensslen, H.-N. Yu *et al.*, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions", *IEEE Journal of Solid-State Circuits*, vol. 9, no. 5, October 1974, pp. 256-268.

[Die82] S. E. Diehl, J. E. Ochoa, P. V. Dressendorfer *et al.*, "Error analysis and prevention of cosmic ion induced errors in CMOS RAM", *IEEE Transactions on Nuclear Science*, vol. 29, no. 6, December 1982, pp. 2032-2039.

[Din77a] A. G. F. Dingwall and R. E. Stricker, "C_2L: A New High-Speed High-Density Bulk CMOS Technology", *IEEE Journal of Solid-State Circuits*, vol. 12, August 1977, pp. 344-349.

[Din77b] A. G. F. Dingwall, R. E. Stricker and J. O. Sinniger, "A High Speed Bulk CMOS C_2L Microprocessor", *IEEE Journal of Solid-State Circuits*, vol. 12, October 1977, pp. 457-462.

[Doy93] Brian S. Doyle, *et al*, "Characterization of Oxide Trap and Interface Trap Creation During Hot-Carrier Stressing of n-MOS Transistors Using the Floating-Gate Technique", *IEEE Electron Device Letters,* vol. 14, No. 2, February, 1993.

[Dre98] P.V. Dressendorfer, Basic mechanism for the new millennium, *Section III of the 1998 IEEE NSREC Short Course,* Newport Beach, 20th July, 1998.

[Duf92] C. Dufour, P. Garnier, T. Carriere and J. Beaucour, "Heavy Ion induced Single Hard Error on sub micronic memories", *IEEE Transactions on Nuclear Science*, vol. NS-39, no. 6, December 1992, pp. 1693-1697.

[Elm82] Y. El-Mansy, "MOS Device and Technology Constraints in VLSI", *IEEE Transactions on Electron Devices*, vol. 29, no. 4, April 1982, pp. 567-573.

[Eng96] Eugene Normand, Boeing Defense & Space Group, "Single Event Upset at Ground Level", *IEEE Transactions on Nuclear Science*, vol.43, No. 6, December 1996.

[Fac99] F. Faccio, *et al*, "Single Event Effects in Static and Dynamic Registers ina 0.25 μm CMOS Technology", *IEEE Transactions on Nuclear Science*, vol.46, No. 6, December 1999.

[Fin] Igor Filanovsky, "Noise of CMOS transistors", EE 633 lecture notes.

[Fot97] D. Foty, "MOSFET modeling with SPICE, Principles and Practice", *Pretice Hall PTR,* Upper Saddle River, New Jersey 1997.

[Fre98] C. Frey, *et al*, "A 1.0V 180Mhz 85 μM/Mhz 8kx16b SRAM in a standard 0.25 μm CMOS", *European Solid-State Circuits Conference* 98.

[Gai95] R. Gaillard, J.-L. Leray, O. Musseau et al., "Techniques de durcissement descomposant, circuits, et systemes electroniques", Notes of the Short Course of the 3rd European Conference on Radiation and its Effects on Components and Systems, Arcachon (France), September 1995, Short Course 3.

[Gel97] C. J. Gelderloos, R. J. Peterson, *et al.*, "Pion-Induced Soft Upsets in 16 Mbit DRM Chips", *IEEE Transactions on Nuclear Science*, vol.44, No. 6, December 1997.

[Gin] Douglas Gingirch, "X-ray Accelerator Facility – description", it can be found at the URL:
http://www.phys.ualberta.ca/~gingrich/atlas/radiation.html

[Gir00] A. Giraldo, A. Paccagnella, A. Minzoni, "Aspect ratio calculation in n-channel MOSFETs with a gate-enclosed layout", *Solid-State Electronics*, vol. 44, 1st June 2000, pp. 981-989.

[Gir98] A. Giraldo, "Evaluation of Deep Submicron Technologies with Radiation Tolerant Layout for Electronics in LHC Environments", Ph.D. Thesis at the University of Padova, Italy, December 1998. It can be found at the URL: http://wwwcdf.pd.infn.it/cdf/sirad/giraldo/tesigiraldo.html

[Gla77] S. Glasstone and P.J. Dolan, The effect of Nuclear Weapons, 3rd ed. Washington, DC: U.S. Dept. of Defenceand U.S. Dept. of Energy, 1977.

[Gri82] P. Grignoux and R. L. Geiger, "Modeling of MOS Transistors with Nonrectangular-Gate Geometries", *IEEE Transactions on Electron Devices*, vol. 29, no. 8, August 1982, pp. 1261-1269.

[Gro84] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. de Keersmaecker, "A reliable approach to charge pumping measurements in MOS transistors", *IEEE Transactions on Electron Devices,* vol. ED-31, p. 42, 1984.

[Has92] A. Hasnain and A. Ditali, "Building-in Reliability: Soft Errors – A Case Study", *Proceeding 30 International Reliability Physics Symposium*, p.276, April 1992.

[Hat85] H. Hatano and K. Doi, "Radiation-tolerant high-performance CMOS VLSI circuit design", *IEEE Transactions on Nuclear Science*, vol. 32, no. 6, December 1985, pp. 4031-4035.

[Hat86] H. Hatano and S. Takatsuka, "Total dose radiation-hardened latch-up free CMOS structures for radiation-tolerant VLSI designs", *IEEE Transactions on Nuclear Science*, vol. 33, no. 6, December 1986, pp. 1505-1509.

[Hen87] W. B. Henley and N. F. Haddad, "Manufacturable Radiation Hardened 1.0 µm CMOS Technology for DoD Applications,"*1987 GOMAC Digest of Papers*, Vol.13, No.1, pp. 115-118, October 1987.

[Hen02] R. Hentschke, F. Marques, F. Lima, L. Carro, A. Susin, R. Reis, "Analyzing area and performance penalty of protecting different digital modules with Hamming code and triple modular redundancy", *Integrated Circuits and Systems Design*, 2002. Proceedings. 15th Symposium on , 9-14 Sept. 2002.

[Hew78] J. Hewitt *et al*, "Ames Collaborative Study of Cosmic Ray Neutrons: Mid-Latitude Flights", *Health Physics,* No. 34, 1978, p. 375.

[Hoh87] J. H. Hohl and K. F. Galloway, "Analytical model for Single Event Burn Out of power Mosfet", *IEEE Transactions on Nuclear Science*, vol. 34, no. 6, December 1987, pp. 1275-1280.

[Hol93] Andrew Holmes-Siedle and Len Adams, "Handbook of Radiation Effects", Oxford University Press, 1993.

[Hsi70] M. Y. Hsiao. "A class of optimal minimum odd-weight-column SEC-DED codes," *IBM J. Res. Develop.* 14, 395-401 (July 1970).

[Hug81] H. L. Huges and R. Razouk, Proc. Electrochem, Society Meeting, 1981.

[Ito95] K. Itoh, K. Sasaki, "Trends in Low-Power RAM Circuit Technology", *Proc. IEEE,* vol. 83, April 1995, pp. 524-543.

[Jar98] P. Jarron, *et al.*, "Deep Submicron CMOS Technologies for the LHC Experiment", presented at the 6th International Conference on Advanced Technology and Particles Physics, October 5-9, 1998, Villa Olmo, Como, Italy.

[Jar99] P. Jarron, G. Anelli, T. Calin *et al.*, "Deep submicron CMOS technologies for the LHC experiments", *Nuclear Physics B (Proceedings Supplements)*, vol. 78, issues 1-3, August 1999, pp. 625-634.

[Joh96] A. H. Johnston, "The Influence of VLSI Technology Evolution on Radiation-Induced Latchup in Space Systems", *IEEE Transactions on Nuclear Science*, vol. 43, no. 2, April 1996, pp. 505-521.

[Joh98] A. H. Johnston, "Radiation Effects in Advanced Microelectronics Technologies", *IEEE Transactions on Nuclear Science*, vol. 45, no. 3, June 1998, pp. 1339-1354.

[Joh99] K. Johansson, M. Ohlsson, N. Olsson, J. Blomgren, and P. Renberg, "Neutron induced single-word multiple-bit upset in SRAM", *IEEE Trans. Nuc. Sci.*, IEEE Computer Society Press, Los Alamitos, Calif, December, 1999.

[Kak86] T. Kakuta, and H. Yaqi, "Irradiation tests of electronic components and materials", 3rd International Workshop on Future Electron Devices, RDA/FED, Tokyo, 1986.

[Kin83] J. H. King, "A novel approach to silicon gate CMOS device scaling", *Solid-State Electronics*, vol. 26, no. 9, 1983, pp. 879-881.

[Klo02] K.Kloukinas, G. Magazzu, A. Marchioro, "A configurable Radiation Tolerant Dual-Ported Static RAM Macro, designed in a 0.26 μm CMOS technology for applications in the LHC environment", 8th workshop on electronics for LHC experiments, September 2002, CERN.

[Lab96] K. A. LaBel and M. M. Gates, "Single-Event-Effect Mitigation from a System Perspective", *IEEE Transactions on Nuclear Science*, vol. 43, no. 2, April 1996, pp. 654-660.

[Lac00] Ronald C. Lacoe, Jon V. Osborn, Rocky Koga, Stephanie Brown, Donals C.Mayer, "Application of Hardness-by-design Methodology to Radiation-Tolerant ASIC Technologies", *IEEE Transactions on Nuclear Science*, vol.47, No.6, p. 2334, December 2000.

[Lam83] J.R. Lamarsh, "Introduction to Nuclear Engineering", Addison-Wesley, Reading, MA.

[Liu92] M. N. Liu, S. Whitaker, "Low power SEU immune CMOS memory circuits", *IEEE Transactions on Nuclear Science*, vol. 39, no. 6, December 1992, pp. 1679-1684.

[LHC] LHC - The larger hadron collider homepage: http://lhc-new-homepage.web.cern.ch/lhc-new-homepage.

[Man02] M. Manghisoni, L. Ratti, V.Re, and V. Speziali, "Submicron CMOS Technologies for Low-Noise Analog Front-End Circuits", *IEEE Transactions on Nuclear Science,* vol 49, No. 6, August 2002.

[Man02a] M. Manghisoni, *et al*, "Radiation Hardness Perspectives for the Design of Analog Detector Readout Circuits in the 0.18-µm CMOS Generation", *IEEE Transactions on Nuclear Science,* vol. 49, No. 6, December 2002.

[May78] T. C. May and M .H. Woods, "A New Physical Mechanism for Soft Errors in Dynamic Memories", *Proceedings of International Reliability Physics Symposium*, p. 33, April, 1978.

[Mcl82] F. B. Mclean and T. R. Oldham, "Charge funneling in N- and P-type substrates," *IEEE Transactions on Nuclear Science*, Vol. NS-29, pp.2018-2023, Dec. 1982.

[Mcw86] P. J. McWorther and P. S. Winokur, "Simple Technique for Separating the Effects of Interface Traps and Trapped-oxide Charge in Metal-Oxide Semiconductor Transistors", *Applied Physics Letters*, vol. 48, no. 2, January 1986, pp. 133-135.

[Mes86] G. C. Messenger and M. S. Ash, "The effects of Radiation on Electronic Systems", Van Nostrand Reinhold, New York, 1986.

[Min84] O. Minato, *et al*, "A 20 ns 64k CMOS Static RAM", *IEEE Journal of Solid-state Circuits,* Vol. sc-19, No. 6, December 1984.

[Moo65] G. E. Moore, "Cramming More Components onto Integrated Circuits", *Electronics*, vol. 38, no. 8, 19 April 1965, pp. 114-117.

[Mul86] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, J. Wiley & Sons, New York, 2nd ed., 1986.

[Nak87] T. Nakamura *et al*, "Altitude Variation of Cosmic Ray Neutrons", *Health Physics,* No. 53, 1987, p.509.

[Nap82] L. S. Napoli, R. K. Smeltzer, R. Donnelly and J. Yeh, "A Radiation Hardened 256*4 Bulk CMOS RAM", *RCA Review*, vol. 43, September 1982, pp. 458-463.

[Nor93] E. Normand and T. J. Baker, "Altitude and Laitude Variations in Avionics SEU and Atmospheric Neutron Flux", *IEEE Transactions on Nuclear Science*, vol. 40, 1993, p.1484.

[Osb98] J. V. Osborn, R. C. Lacoe, D. C. Mayer and G. Yabiku, "Total Dose Hardness of Three Commercial CMOS Microelectronics Foundries", *IEEE Transactions on Nuclear Science*, vol. 45, no. 3, June 1998, pp. 1458-1463.

[Pet] E. L. Petersen and P. W. Marshall, "Single event phenomenon in the space and SDI arenas", Naval Research Lab. (NRL) Tech. Presentation.

[Pfi85] J. R. Pfiester, J. D. Shott and J. D. Meindl, "Performance Limits of CMOS ULSI", *IEEE Transactions on Electron Devices*, vol. 32, no. 2, February 1985, pp. 333-343.

[RD49a] P. Jarron, G. Anelli *et al.*, 2nd RD49 Status Report, "Study of the Radiation Tolerance of IC's for LHC", CERN/LHCC/99-8, LEB Status Report/RD49, 8 March 1999.

[RD49b] P. Jarron, G. Anelli *et al.*, 3rd RD49 Status Report, "Study of the Radiation Tolerance of IC's for LHC", CERN/LHCC/2000-003, LEB Status Report/RD49, 13 January 2000.

[Rei82] G. Reimbold and P. Gentil, "White Noise of MOS Transistors Operating in Weak Inversion", *IEEE Transactions on Electron Devices*, vol. 29, no. 11, November 1982, pp. 1722-1725.

[Rei83] A. Reisman, "Device, Circuit, and Technology Scaling to Micron and Submicron Dimensions", *Proceedings of the IEEE*, vol. 71, no. 5, May 1983, pp. 550-565.

[Roc88] L. R. Rockett, "An SEU-hardened CMOS data latch design", *IEEE Transactions on Nuclear Science*, vol. 35, no. 6, December 1988, pp. 1682-1687.

[RPC90] "Radiation Processing: state of art". Proceedings of 7th International Meeting on Radiation Processing. *Radiation Physics and Chemisrty, International Journal of Radiation applications and instrumentation*, part C, 35(1-6).

[Sak84] T. Sakurai, *et al*, "A Low Power 46 ns 256 kbit CMOS Static RAM with Dynamic Double Word line", *IEEE Journal of Solid State Circuits*, vol. sc-19, No.5, october, 1984.

[Sak86] N. S. Sakes, N. G. Ancona, J.A. Molodo, "Generation of Interface States by Ionizing Radiation in Very Thin MOS Oxides", *IEEE Transactions on Nuclear Science,* vol.33, P.1185, December 1986.

[Sav98] J. Savir, "Redundancy revisited [CMOS combinational circuits]", *Instrumentation and Measurement Technology Conference*, IMTC/98, Conference Proceedings, IEEE , Vol. 1, 18-21, May 1998.

[Sch90] D. K. Schroeder, "Semiconductor Material and Device Characterization", New York: Wiley, 1990.

[Sel87] P. Seller, "The Matching Condition for Optimum Thermal Noise Performance of F.E.T. Charge Amplifiers", *Rutherford Appleton Laboratory*, September 1987.

[Sex85] F. W. Sexton and J. R. Schwank, "Correlation of Radiation Effects in Transistors and Integrated Circuits", *IEEE Transactions on Nuclear Science*, vol. 32, no. 6, December 1985, pp. 3975-3981.

[Sex97] F. W. Sexton, D. M. Fleetwood, M. R. Shaneyfelt et al., "Single Event Gate Rupture in Thin Gate Oxides", *IEEE Transactions on Nuclear Science*, vol. 44, No. 6, December 1997, pp. 2345-2352.

[Sha98] M. R. Shaneyfelt, P. E. Dodd, B. L. Draper and R. S. Flores, "Challenges in Hardening Technologies Using Shallow-Trench Isolation", *IEEE Transactions on Nuclear Science*, vol. 45, December 1998, pp. 2584-2592.

[Shi83b] H. Shichijo, "A re-examination of practical performance limits of scaled nchannel and p-channel MOS devices for VLSI", *Solid-State Electronics*, vol. 26, no. 10, 1983, pp. 969-986.

[SIA99] *The International Technology Roadmap for Semiconductors*, 1999 Edition. The document is sponsored by the Semiconductor Industry Association (SIA), the European Electronic Component Association (EECA), the Electronic Industries Association of Japan (EIAJ), the Korean

Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA), and can be found at the URL: http://notes.sematech.org/ntrs/Rdmpmem.nsf.

[Sno00] W. Snoeys, G. Anelli, M. Campbell *et al.*, "Integrated Circuits for particle physics experiments", *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, December 2000.

[Soo85] Lal C. Sood, *et al*, "A Fast 8Kx8 CMOS SRAM With Internal Power Down Design Techniques", *IEEE Journal of Solid-State Circuits,* vol. sc-20, No. 5, October 1985.

[Spj83] W. N. Spjeldvik and P. L. Rothwell, "The Earth's radiation belts," AFGL-TR-83-0240, Air Force Geophysics Lab, Hanscom AFB, MA, Sept.29, 1983.

[Sro03] J. R. Srour, C. J. Marshall, P. W. Marshall, "Review of Displacement Damage Effects in Silicon Devices", *IEEE Transactions on Nuclear Science,* Vol. 50, Issue: 3, June 2003, pp. 653 – 670.

[Sta88] E.G. Stassinopulos, J.P. Raymond, "The Space Environment for Electronics", *Proceedings of the IEEE*, vol. 76, Issue 11, Nov. 1988, pp1423-1442.

[Ted92] S. Tedja, *et al.*, "Noise Spectral Density Measurements of a Radiation-hardened CMOS Process in the Weak and moderate Inversion", *IEEE Transactions on Nuclear Science*, vol. 39, no. 4, 1992, pp. 804-808.

[Tsi99] Y. Tsividis, *Operation and Modeling of The MOS Transistor*, Second Edition, McGraw-Hill International Editions, 1999.

[Tur02] *B. N. Turman, R. J. Kaye, J. A. Jacobs,* "An Overview of Electron Beam Decontamination Technology and Applications", *Power Modulator Symposium, 2002 and 2002 High-Voltage Workshop, Conference Record of the Twenty-Fifth International*, 30 June-3 July 2002, pp. 39 – 43.

[Val94] R.Velazco, D. Bessot, S. Duzellier, R. Ecoffet, R. Koga, "2 CMOS Memory Cells Suitable for the Design of SEU-Tolerant VLSI Circuit", *IEEE Transactions on Nuclear Science,* vol. 41, No.6, p.2229, December 1994.

[Van91] G. Van den Bosh, G. V. Groeseneken, P. Heremans, and H. E. Meas, "Spectroscopic charge pumping: A new procedure for measuring interface interface trap distributions on MOS transistors," *IEEE Trans. Electron Devices,* vol. 38, p. 1820, 1991.

[Vel94] R. Velazco, D. Bessot, S. Duzellier *et al.*, "Two CMOS Memory Cells Suitable for the Design of SEU-Tolerant VLSI Circuits", *IEEE Transactions on Nuclear Science*, vol. 41, no. 6, December 1994, pp. 2229-2234.

[Vit96] E. A. Vittoz, Notes of the Advanced Engineering Course on CMOS & iCMOS IC Design, Lausanne, Switzerland, 19-23 August 1996.

[VLS82] VLSI Laboratory, Texas Instruments Inc., Dallas (Texas, USA), "Technology and Design Challenges of MOS VLSI", *IEEE Journal of Solid-State Circuits*, vol. 17, no. 3, June 1982, pp. 442-448.

[Wal00] S. Wald, A. Pokryvailo, G. Appelbaum, M. Katz, E. I. Weiss, "Hazardous Waste Treatment and Recovery of Valuable Products With a Thermal Pulsed-Plasma Technology", *IEEE Transactions on Plasma Science,* Vol. 28, Issue: 5, Oct. 2000, pp. 1576 – 1580.

[Wea87] H. T. Weaver, C. L. Axness, J. D. McBrayer *et al.*, "An SEU tolerant memory cell derived from fundamental studies of SEU mechanisms in SRAM", *IEEE Transactions on Nuclear Science*, vol. 34, no. 6, December 1987, pp. 1281-1286.

[Whe94] C. F. Wheatley, J. L. Titus and D. I. Burton, "Single Event Gate Rupture in vertical power MosFets, an original empirical expression", *IEEE Transactions on Nuclear Science*, vol. 41, no. 6, December 1994, pp. 2152-2160.

[Whi91] S. Whitaker, J. Canaris, K. Liu, "SEU hardened memory cells for a CCSDS Reed-Solomon encoder", *IEEE Transactions on Nuclear Science*, vol. 38, no. 6, December 1991, pp. 1471-1477.

[Whi93] M. White, B. Bartholet, and M. Baze, "Automated Radiation Hard ASIC Design Tool", in Proceedings of the 5th NASA Symposium on VLSI Design, p. 11.4.1-11.4.8, Albuquerque, New Mexico, November 1993.

[Wis93] D. Wiseman, J. Canaris, S. Whitaker *et al.*, "Design and testing of SEU/SEL immune memory and logic circuits in a commercial CMOS process", *Workshop Record of the 1993 IEEE Radiation Effects Data Workshop*, July 1993, pp. 51-55.

[Yos83] M. Yoshimoto, *et al*, "A 64kb CMOS RAM with Divided Word line Structure", *ISSC Dig. of Tech Papers,* pp 58-59, Feb. 1983.

[Yu79] H.-N. Yu, A. Reisman, C. M. Osburn and D. L. Critchlow, "1 μm-MOSFET VLSI Technology: Part I – An Overview", *IEEE Transactions on Electron Devices*, vol. 26, no. 4, April 1979, pp. 318-324.

[Zie96] J. F. Ziegler *et al*, "IBM Experiments in Soft Fails in Computer Electronics (1979-1984)", *IBM J. Res. Develop*, 40, 1996, pp.3.